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Phase-5 Tests and Studies of the Run IIa Analog Front End Board

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Acknowledgments

We would like to acknowledge John Anderson, Fred Borcherding, Stefan Grunendahl, George Ginther, Marvin Johnson and Paul Rubinov. Without their work on the AFE board, the phase-5 AFE tests and analysis described here would not have happened.

Abstract

Each of the 198 Analog Front End Boards that instrument the Central Fiber Tracker and the Pre-shower Detectors were thoroughly tested in the Phase-5 test stand and certified prior to commissioning in the Run IIa D0 detector. We describe those tests and discuss the online and offline analysis of the data taken on the test stand. We present a variety of results on the SVX gains, discriminator turn-on and gains and pedestal behavior. We also discuss the board certification issues for commissioning and show distributions that provide a global perspective of the system. Complete results from the analysis are stored at http://www-d0.fnal.gov/d0dist/dist/packages/afe_phase5/.

Contents

1. Introduction

The Analog Front End (AFE) Boards instrument three Scintillation Fiber detectors, the Central Fiber Tracker (CFT), the Central Pre-Shower (CPS) and the Forward Pre-Shower (FPS), in the D0 detector. They receive charge signals from the fibers via the Visible Light Photon Counters (VLPCs) and provide (1) digital output for the trigger and (2) analog signals. The AFE board also provides VLPC bias and temperature control functionalities.

There are three (color-coded) versions of the AFE board, which differ from each other in input gain and VLPC bias control circuitry. The details are as follows:

- CFT boards – "green" – 136 needed (76 for axial layers/trigger)
- CPS/CFT boards – "blue" – 30 needed (10 for axial layers/trigger)
- FPS boards – "red" – 32 needed (all needed for trigger)

(Note: However, some "blue" boards are CFT only.)
Between the three versions of the AFE boards, they instrument the 77,000 channels of the CFT, 7,680 channels in the CPS and 14,000 channels in the FPS.

The AFE boards also have a handedness. There are Left-handed (LH) and Right-handed (RH) boards because of the way the boards are installed on VLPC cassettes. Each AFE board has eight Multi-Chip-Modules (MCMs) and each MCM instruments a total of 64 channels with both analog and digital outputs. Each MCM has 1 Silicon Vertex (SVX-IIe) charge-sensitive ADC (72 bonded channels out of a total of 128; 64 get used) and 4 SIFT (Scintillating Fiber Trigger) discriminator chips (64 total channels- 2 SIFTs with 14 channels and 2 with 18 channels). A photograph of an RH AFE board is shown in Fig. 1, with important components labeled. For detailed design specifications see Ref. 1. Other notable sub-systems apart from the eight MCMs are:

- 1553 Control & Communication systems
- A "virtual SVX" (VSVX) system to buffer discriminator data for readout with SVX data
- A high-speed data multiplexing system which routes all discriminator data from the VSVX via LVDS links to Digital Front End (DFE) boards.
- Analog monitoring for the VLPC temperature and bias (bias & cryo control)
- DAC system to develop all control voltages for SIFTs
- A clock generation system to generate all timing clock pulses for the SIFTs

All major logic functions are provided using Complex Programmable Logic Devices (CPLDs). Embedded software in the on-board microprocessor is used to respond to commands from the external world that appear on the 1553 bus.

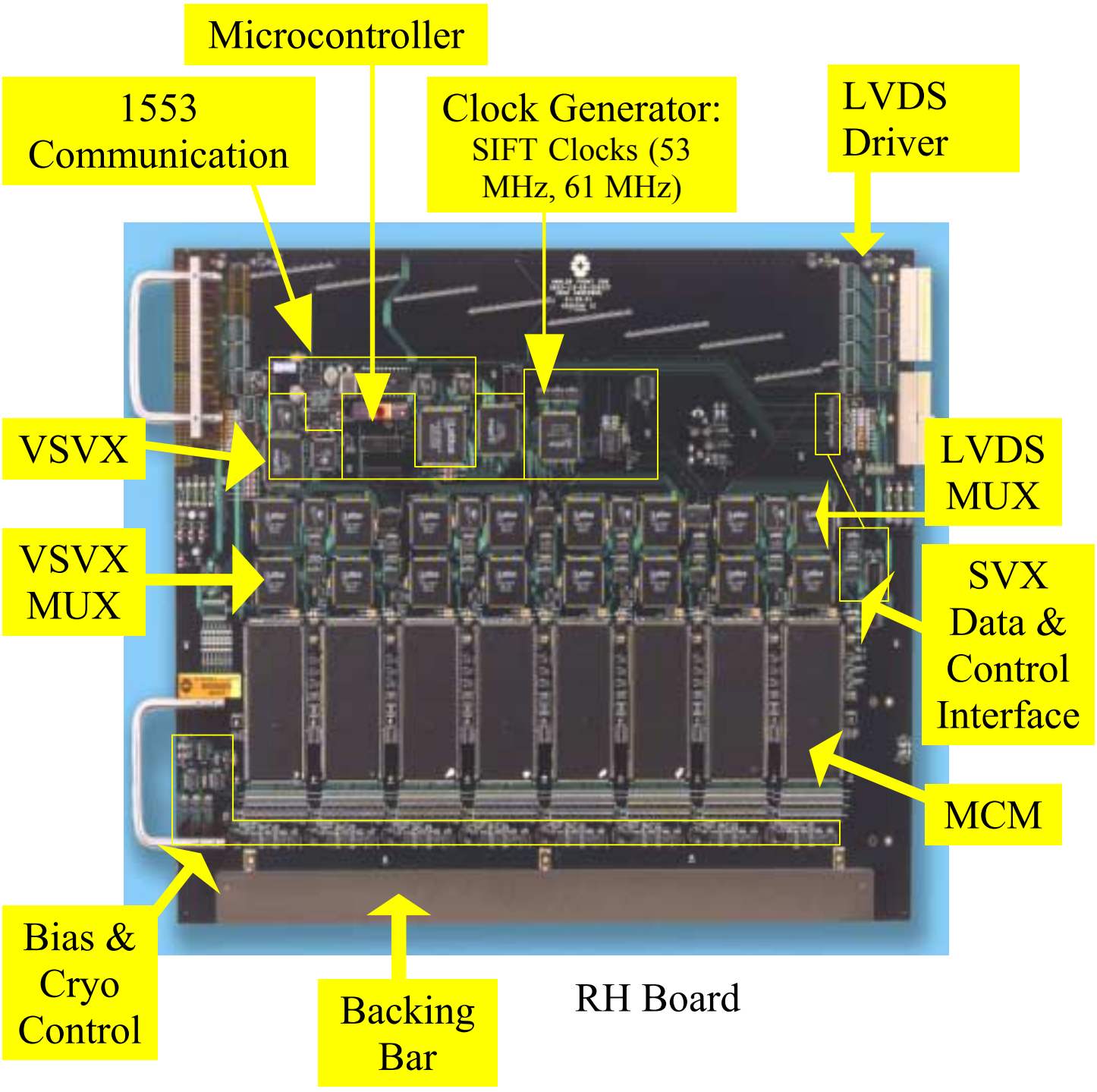


Fig. 1: A photograph of a Right-handed AFE Board

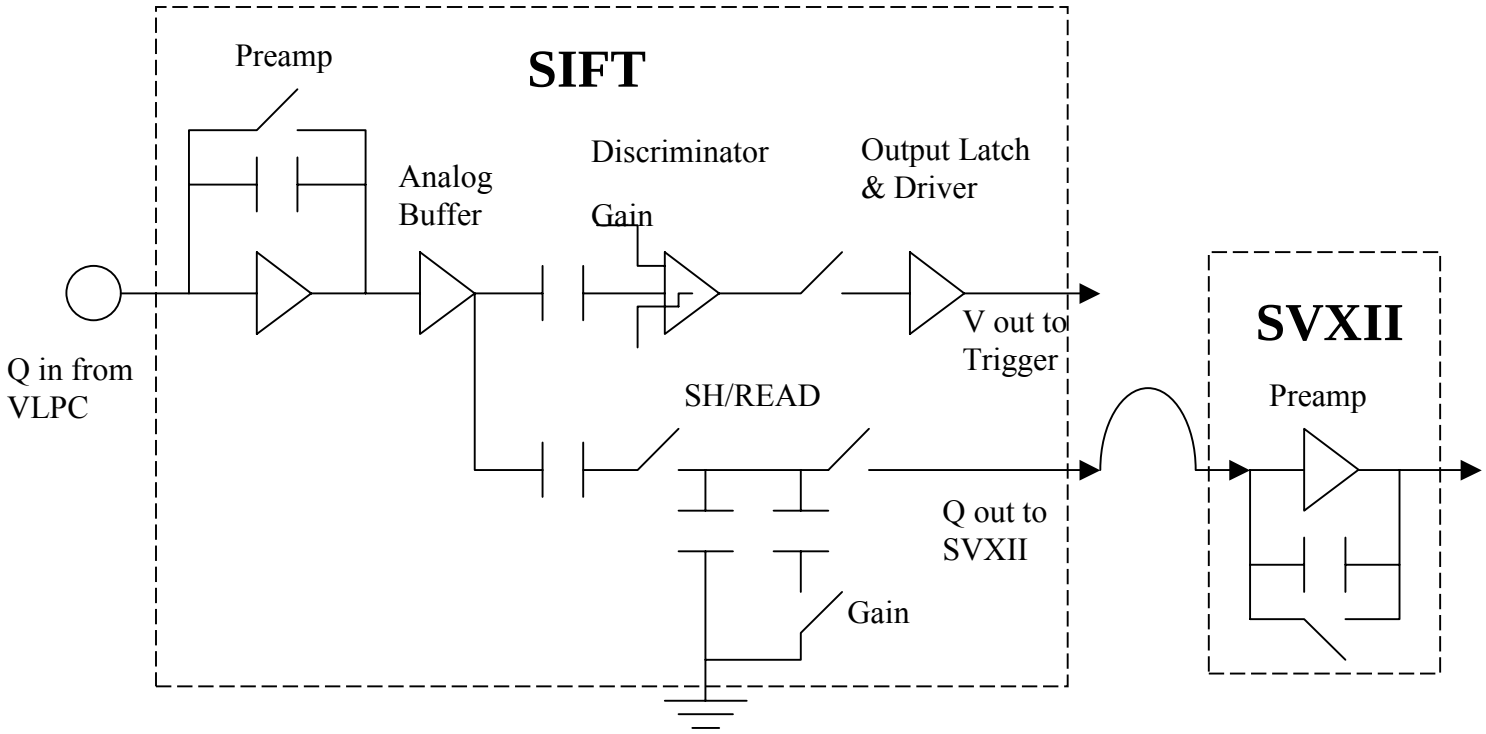


Fig. 2: Simplified schematic of a single channel of the MCM. Each analog input is routed to a SIFT channel where it is discriminated for a voltage output and integrated and passed onto an SVX2e chip input channel. The output of the SVX2e is a digitized amplitude.

2. Phase-5 Test Goals

The phase-5 test of the AFE checks all functional aspects of every AFE board and it is used to evaluate the AFE's readiness for installation in the detector on the platform. The primary goals of the phase-5 testing are:

1. Re-testing the basic functionalities of the devices (communication interfaces, microcontroller, SVX and SIFTs),
2. Testing and studying the response of all 512 channels of the AFE to injection of charge,
3. Testing the ability of the AFE to operate the bias voltage and cryogenic temperature control systems, and
4. The verification of the transfer of discriminator information to the level-1 trigger system.

If the Phase-5 test results are satisfactory (see description in Sec. 6), the board is ready for testing on a combined test stand (a final integration test) and then installed in the detector. If not, repairs are made and the board is re-tested and re-evaluated.

3. Phase-5 Test Stand and Data Acquisition

To accomplish the primary goals of Phase-5 testing, an Analog Front End Test Module (AFETM) was designed and built. An AFETM is connected to the AFE by means of 8 VLPC 64 channel flex cables (V64), just as the AFE would be connected to the Visible Light Photon Counters (VLPC) when installed in the cassette located under the D0 detector. Circuitry located on the AFETM is capable of injecting variable and programmable amounts of charge into the conductors located on the V64 cables and thus into the AFE. Also located on the AFETM is circuitry used to emulate the response of the cryogenic temperature monitoring resistors that are located under the VLPCs as well as circuitry that can verify the operation of both the cryogenic temperature and bias voltage control circuits on the AFE.

These aspects of the Phase-5 testing of the AFE are incorporated into Visual Basic (VB) code (running under Excel) that controls the hardware used to generate the test stimuli. The code also reads the AFE and AFETM for the results. The test hardware (except for the AFETM) resides in a VME crate located in the rack that holds the AFE backplane structure. The computer, which runs the VB code, communicates with the VME crate via a Bit3 card and cable system. Within the VME crate is the 1553 Controller that sends instructions to and reads some test results back from the AFE and the AFETM. Also within the VME crate is the Stand Alone Sequencer (SASEQ) that is used to read Level 3 data from the AFE. To test the response of channels on the AFE, the VB code sends 1553 commands to the VME crate through the Bit3 system. The 1553 controller interprets the commands and sends (or receives as necessary) appropriately coded 1553 compliant communication to either the AFE or the AFETM, to; set various Digital to Analog Converters (DACs), configure patterns of channels to inject charge to, set or clear various digital signal levels, etc. The VB code then instructs the SASEQ (again using the Bit3 system) to initiate a data transfer cycle, then reads the resulting AFE digitized charge information and discriminator output information back from the SASEQ. Typically, many events are taken for a given set up. For each channel on the AFE, the mean of the digitized charge value and the occupancy of the discriminated output is computed and compared to limits. If the AFE is capable of performing the base level operations and the channel response falls within limits, more extensive characterization tests are run and analyzed off-line.

To test the generation and transfer of trigger inputs, a module used to verify the design of the Digital Front End (DFE) module is used to read and verify the Level 1 Trigger information from the AFE. The Data Pump module can accept a stream of Low Voltage Differential Signals (LVDS) from the AFE and make it available to the computer running the test. The AFE forms LVDS data streams from the discriminator output data from the MCMs and would send the data to the DFE in normal running mode. Code installed in some of the Complex Programmable Logic Devices (CPLD) on the AFE boards can generate known patterns of diagnostic discriminator data to the LVDS drivers when instructed to do so.

The LVDS portion of the Phase 5 test is run using a different VB code than discussed in an earlier part of this section. The same path to the VME crate is utilized, but as noted above, the data comes from the Data Pump module instead of the SASEQ. The data format is sufficiently different and the LVDS test code was written late enough that no effort was made to integrate both tests into a common package.

4. Phase-5 Tests

The tests conducted on the AFE boards during phase-5 fall into three categories:

1. Retesting some of the basic functionalities of the AFE board even though they were looked at in earlier phases of testing:

    - The AFE can respond to the 1553 communication system
    - The microcontroller is working
    - The chain of SVX chips are functional and respond to commands
    - The discriminators are functional

2. Testing the response of all 512 channels of the AFE to charge injection:

    1. Establish the operating voltage V_{ref} (V_{ref} scan)
    2. SVX response for different amounts of charge injected $\Rightarrow$ SVX gain
    3. Discriminator threshold scans with different amounts of charge injected
    4. SIFT gain $\Rightarrow$ Discriminator turn-on curve
    5. Pulse channels in different patterns and readout
    6. Pedestals (means and sigmas) for all channels

3. Testing the ability of the AFE to operate the bias voltage and cryogenic temperature control

5. Test Stand Data and Analysis

Channel level testing of the AFE Module at the Phase-5 test stand is carried out in two sections, the V_{ref} sweep and the online analysis, followed by a section that generates data for off-line analysis. The goal of the V_{ref} sweep section is to determine an appropriate voltage to apply to each SIFT as an operating parameter. The online test and analysis procedure injects charge into AFE analog input channels in an attempt to determine to what extent all channels are responding but not to the detail attempted in the off-line testing.

The AFE Test Module (AFETM) is designed to allow the injection of a variable amount of charge into the analog input channels of the AFE. The design allows the injection of charge into as few as 8 non-adjacent (but common to a single Multi-Chip Module (MCM)) channels at a time.

The AFE test stand code operates in a series of steps. The code processes each step by first reading an array of stored test parameter values, writing these values to appropriate registers and Digital-to-Analog Converters (DACs) on both the AFE and the AFETM to set up a given step in the test. The system is then triggered and data (both discriminator and digitized) are read out from the AFE for a number of events for each step. The data read from the AFE are stored by channel into three arrays after discriminator occupancy, SVX mean and SVX standard deviation calculations are computed. The V_{ref} scan operates under this arrangement changing the V_{ref} DAC values in steps. The other On-line tests as well as those associated with the generation of data for the offline test use the constant values for the V_{ref} DACs as determined from the V_{ref} scan, but vary other parameters depending on what is to be tested.

5.1. V_{ref} Scan

The V_{ref} input to the SIFT is used to match the quiescent SIFT output capacitor voltage to the SVX input offset voltage. Differences in these voltages are seen as charge by the SVX and can be either positive or negative depending on the sign of the difference. Note that this charge is due to the operation of the SIFT chip and not due to charge injected into a SIFT input channel. For very small values of the V_{ref} input voltage, the difference between the SIFT and SVX is large and negative (the capacitor output voltage is less than the SVX channel input voltage). The effective negative charge transferred to the SVX is sufficient to saturate the SVX. At the maximum voltage of the V_{ref} input, the difference is large and positive. The effective positive charge transferred to the SVX is also sufficient to saturate the SVX. The mean value of all saturated bonded SVX channels is a constant value, dependent on the initialization values downloaded to the SVX chip. As the voltage of the V_{ref} input is increased, the SVX channels start to come out of saturation and respond to the small negative charge with mean values of less than the saturated value. As the V_{ref} input voltage continues to increase, the effective negative charge applied to the SVX input decreases and the mean value of the SVX channels falls to zero. At some V_{ref} input voltage, the SIFT output capacitor voltage and the SVX input voltages are equal. Increasing the V_{ref} voltage past this point results in the effective transfer of positive charge into the SVX. At some greater V_{ref} voltage, the amount of positive charge injected into the SVX results in the channel mean to start to rise from zero. The mean values of the SVX channels increase linearly with increasing V_{ref} input voltage (stored as a DAC value by the code) until the SVX approaches saturation and the mean drops to the constant saturation value.

In the V_{ref} sweep, the DACs that drive the V_{ref} input to each of the 32 SIFT chips located inside the MCMs located on the AFE, are swept in 1 count steps through a portion of their range such that the lower and upper saturation ranges of the SVX channels can be observed. For each step of the V_{ref} sweep, the AFE is triggered 20 times and the mean response for each of the 512 channels on the AFE is calculated and stored in an array. After all 58 steps that comprise the V_{ref} sweep are completed, the Visual

Basic code that runs the AFE testing computes appropriate V_{ref} values for each SIFT. Component variations do not allow the establishment of a single global value for this voltage.

Each channel responds slightly differently to the V_{ref} sweep. With one V_{ref} input for each SIFT, and a single SIFT controlling 18 channels, the code attempts to determine the best V_{ref} DAC value for each SIFT. This is accomplished first on an individual channel basis, then by grouping the results by SIFT and selecting the average value calculated from all channels associated with a given SIFT. If channel responses are widely divergent, the code may determine that a V_{ref} value is not calculable and generate an error. The method the code uses to determine the V_{ref} DAC value is to look for the V_{ref} DAC value at which the SVX channel mean first exceeds the saturation value by a fixed amount. In practice, this offset (10 counts used in our tests) would be chosen in an attempt to equalize the bonded channels at a common pedestal value and to allow the differentiation of bonded from unbonded or unused channels. Once the V_{ref} DAC value for each SIFT had been determined, it is stored in an array for future reference.

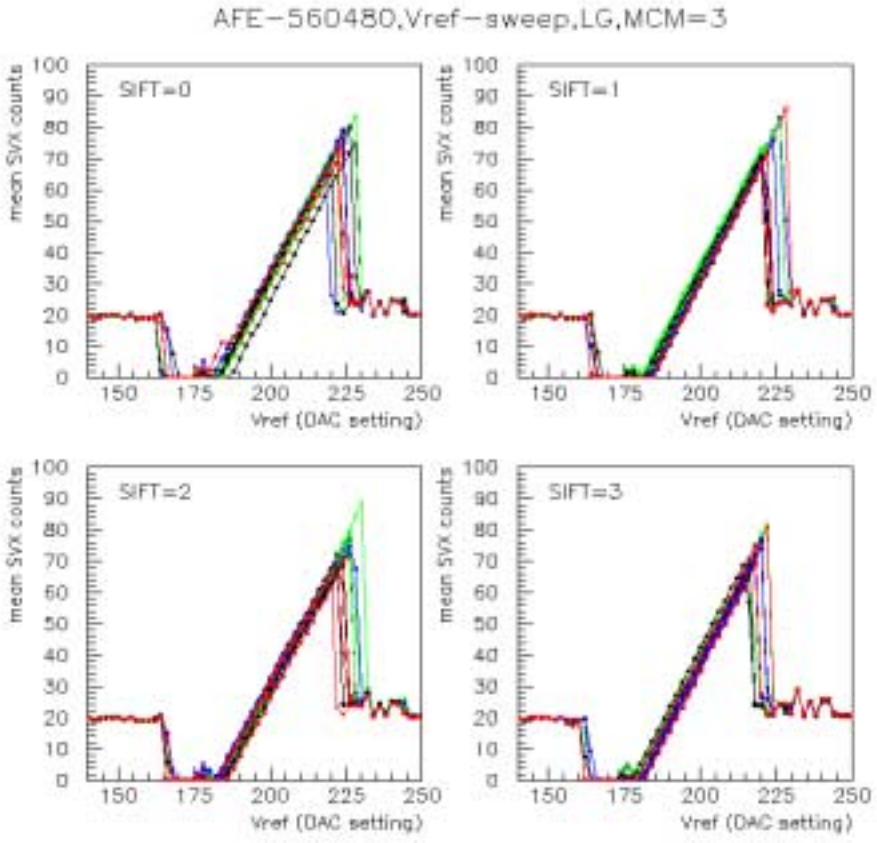


Fig. 3: V_{ref} Scan: Plots of mean SVX response for each SVX channel in each SIFT (one plot/SIFT) of an MCM for AFE Board 560480, as a function of the applied reference voltage.

5.2. Other Online Tests

In the online analysis procedure, the test stand code instructs the AFETM to inject charge into all 512 channels on the AFE in 8 steps, applying the same charge to the same 8 channels in each of the 8 MCMs on each step. For each of these steps, the test stand code stores discriminator and SVX data for 500 events.

With the V_{ref} DAC values as determined in the V_{ref} sweep loaded into the parameter array, the amplitude of the digitized signal found for channels into which charge has been injected is expected to be relatively constant across all SIFT channels. The amount of charge injected into each channel (implemented in the parameter array as the value written to a DAC on the AFETM) was empirically selected to result in something less than full-scale response from the SVX for the initialization values downloaded to the SVX. The mean value obtained for each of the 1024 SVX channels on the AFE is compared to limits to gauge the response of the channel. Since not all channels are subjected to charge injection on each of the 8 steps, the test stand code considers channels to be of one of four types for each step. There are 56 channels on each SVX that are not connected to any input, these are considered to be non-bonded channels. There are 8 channels on each MCM that are fully instrumented but not connected to an analog input channel on the AFE; these are unused channels. The remaining 512 SVX channels are fully instrumented on the MCMs and are connected to analog input channels on the AFE. Only 64 are capable of receiving charge from the AFETM at a time for a given step, these are considered pulsed channels. The channels not receiving charge for a given step are non-pulsed channels. For each step in the On-line test section, all SVX channels are subjected to different limits depending on what kind of channels they are. Channels with mean values outside the established limits are flagged as failed.

At the same time that channels are subjected to injected charge for determination of their mean SVX values, the discriminator function of each of the channels is also being tested. There are 512 discriminated outputs from the MCMs on the AFE. They are divided into pulsed and unpulsed categories for each step depending on which ones are receiving the charge from the AFETM. For the evaluation of the discriminator channels on the AFE, the test stand code computes the fraction of times a discriminator channel was found to be ON (charge found to be in excess of threshold). Correctly responding discriminator channels should have occupancy of no less than 1 when they are being pulsed and no more than 0 when they are not being pulsed. Circuitry on the AFE exists to apply an effective threshold voltage to the SIFT chips for use in the charge discrimination operation. These threshold voltages can be changed by writing to DACs located on the AFE. The values to be written to the threshold DACs are stored in the parameter array for each test step. The particular values to be written to the threshold DACs (setting the charge threshold level for discriminator operation) were chosen empirically based on the amount of charge injected for the SVX channel testing.

5.3. Pedestals

The pedestals were read out multiple times (~100-300) and the pedestal mean and sigma for each channel were stored in the data files for offline analysis. The pedestal means and sigmas for a typical board are shown in Fig. 4. The distributions of the same are shown in Fig. 5. The pedestal sigma was required to be within 7 ADC counts (or 1 p.e.) in the low gain (LG) mode for the channel to be tagged as a good channel. We have performed some zero suppression studies using the pedestal data both from phase-5 test data and some data taken on the platform. These are discussed in section 5.6.

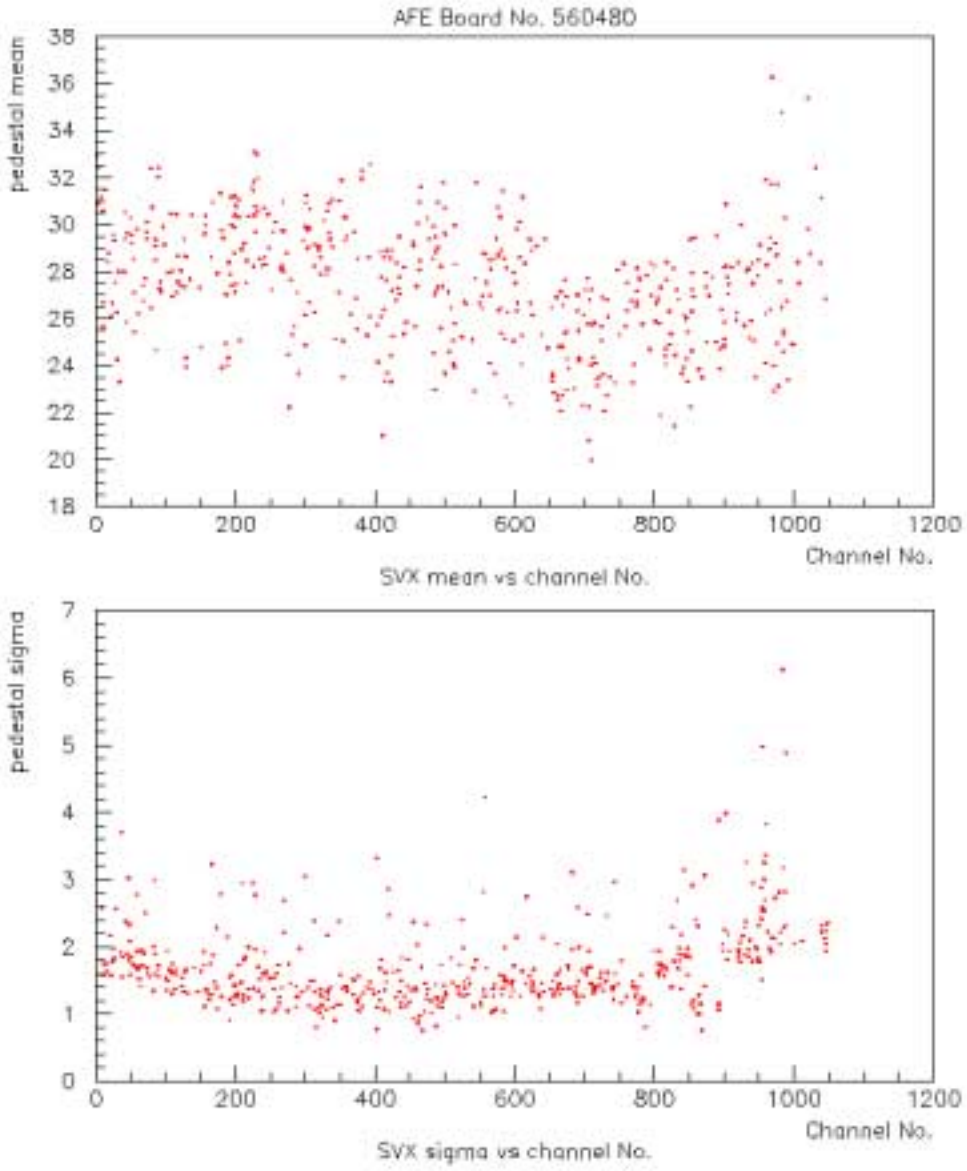


Fig. 4: Pedestal means and sigmas for each of the 512 channels for AFE board 560480

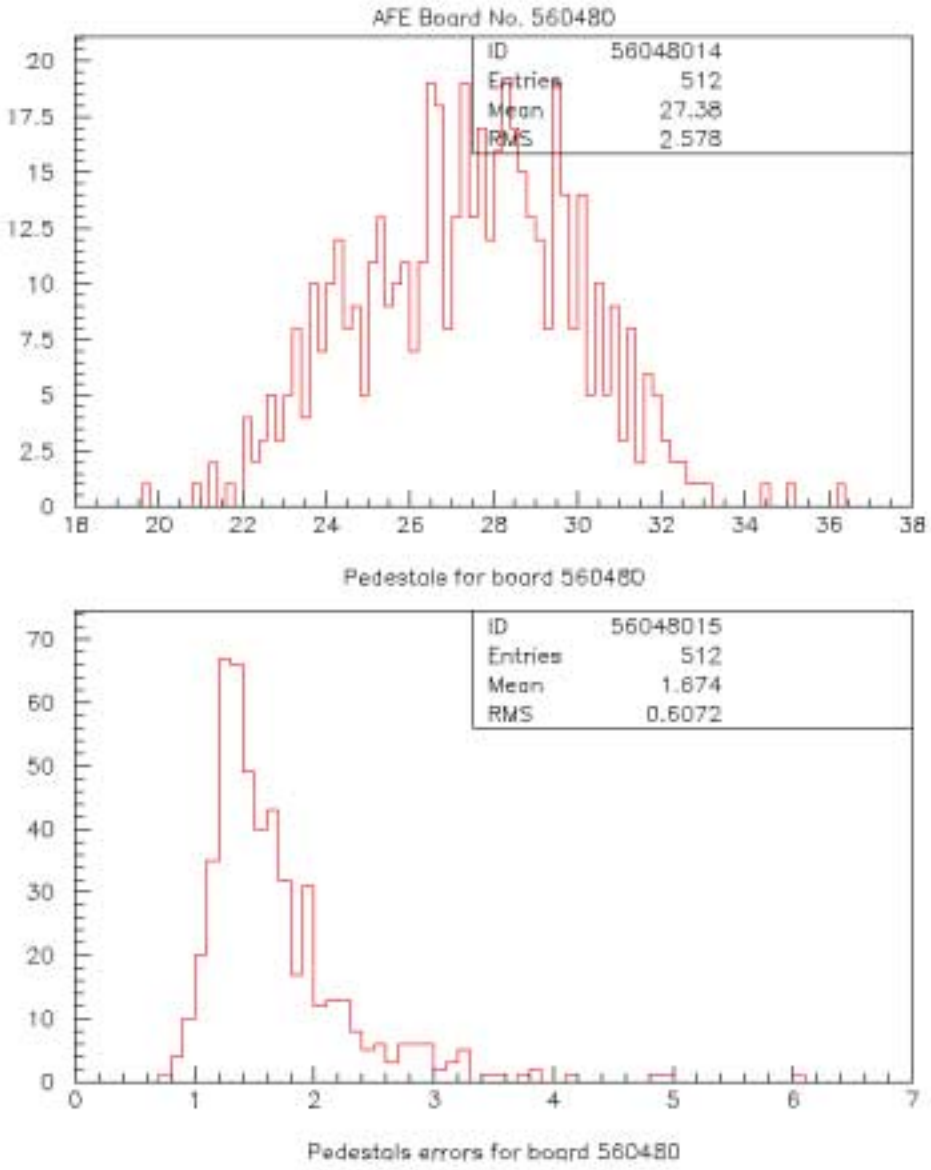
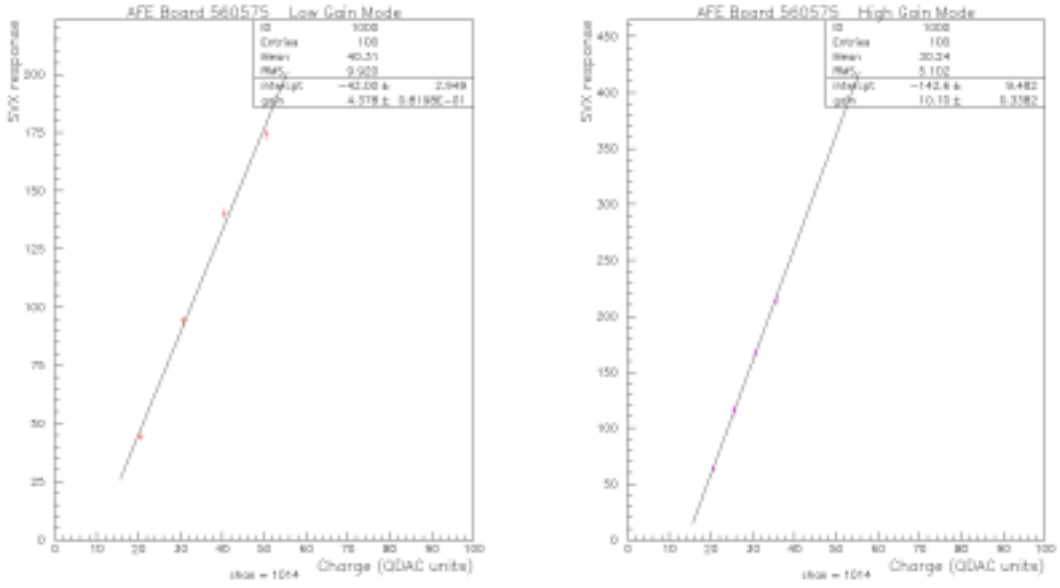


Fig. 5: Distributions of pedestal means and sigmas for AFE board 560480.

5.4. SVX Response and SVX Gain Studies

During the tests, pre-determined amounts of charges (Q = 20, 30, 40, 50 QDAC units, 1QDAC unit ≈ 4.5 fC) are injected into each of the SVX channels and the response read out. This was done both in the "Low Gain" (LG) and "High Gain" (HG) modes. For each channel, then, we perform a linear fit (using MINUIT in PAW) to the SVX response as a function of the input charge to determine the SVX gain for that channel. Fig. 6 (a) and (b) show such a linear fit for one of the channels in low gain and high gain modes, respectively. The gains and offsets from the fits for all pulsed channels are shown in Figs. 7 and 9. The distributions of gains and offsets are shown in Figs. 8 and

10. The average SVX gain for the AFE board 560575 in low-gain mode is 4.766 ADC counts/QDAC unit and in high gain mode is 9.95. (One photoelectron, 1 p.e., corresponds to about 7 counts in the LG mode and about 15 counts in the HG mode). The ratio of SVX gain in HG mode to LG mode is ~ 2.1 for the board 560575. The distribution of gain for all installed boards are discussed later.



(a) **(b)**

Fig. 6: SVX response in ADC units as a function of injected charge (in QDAC units) for channel number 1014 in Low Gain mode (Left) and High Gain mode (Right).

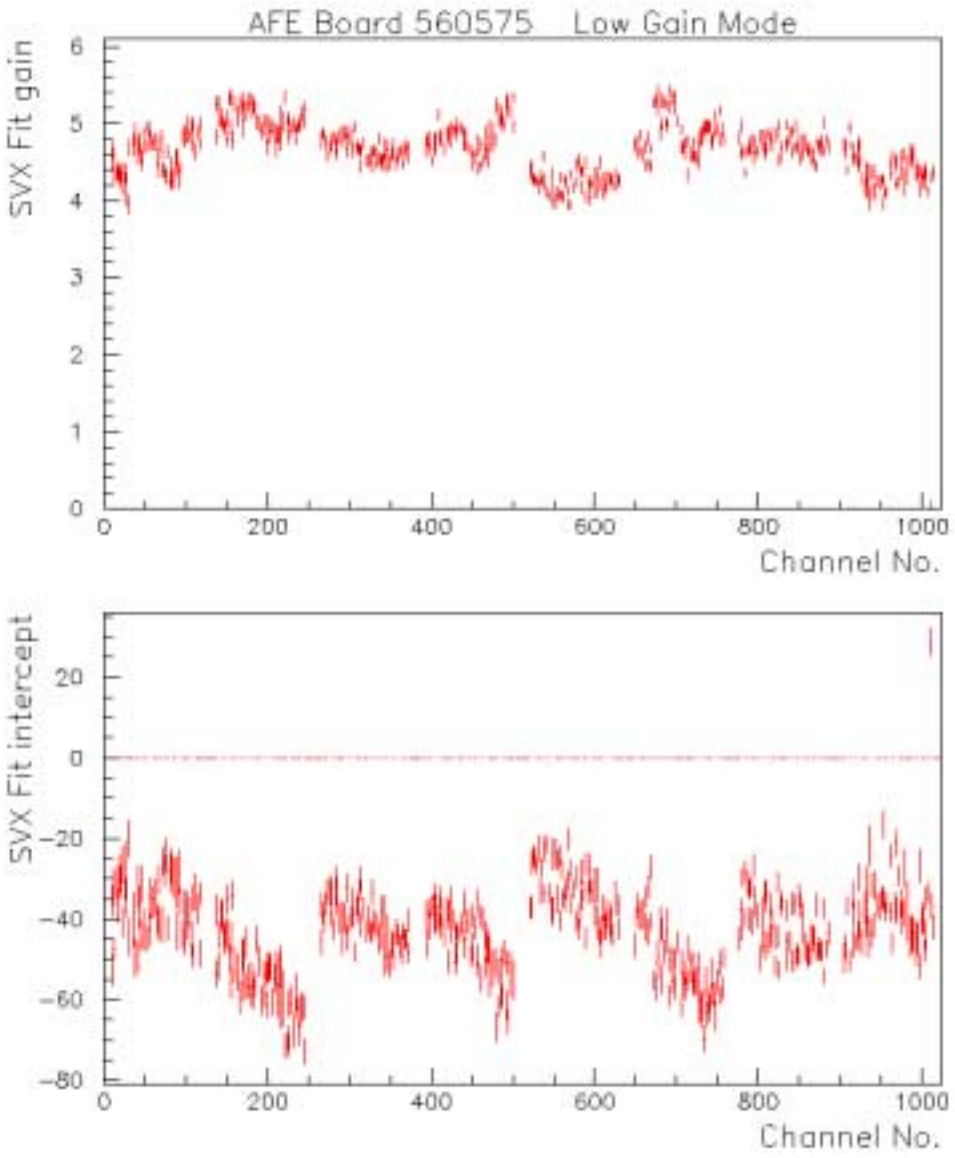


Fig. 7: Results of linear fits to SVX response vs. charge for all 512 channels in Low Gain mode. (Top) Fitted SVX Gain, (Bottom) Fitted offset.

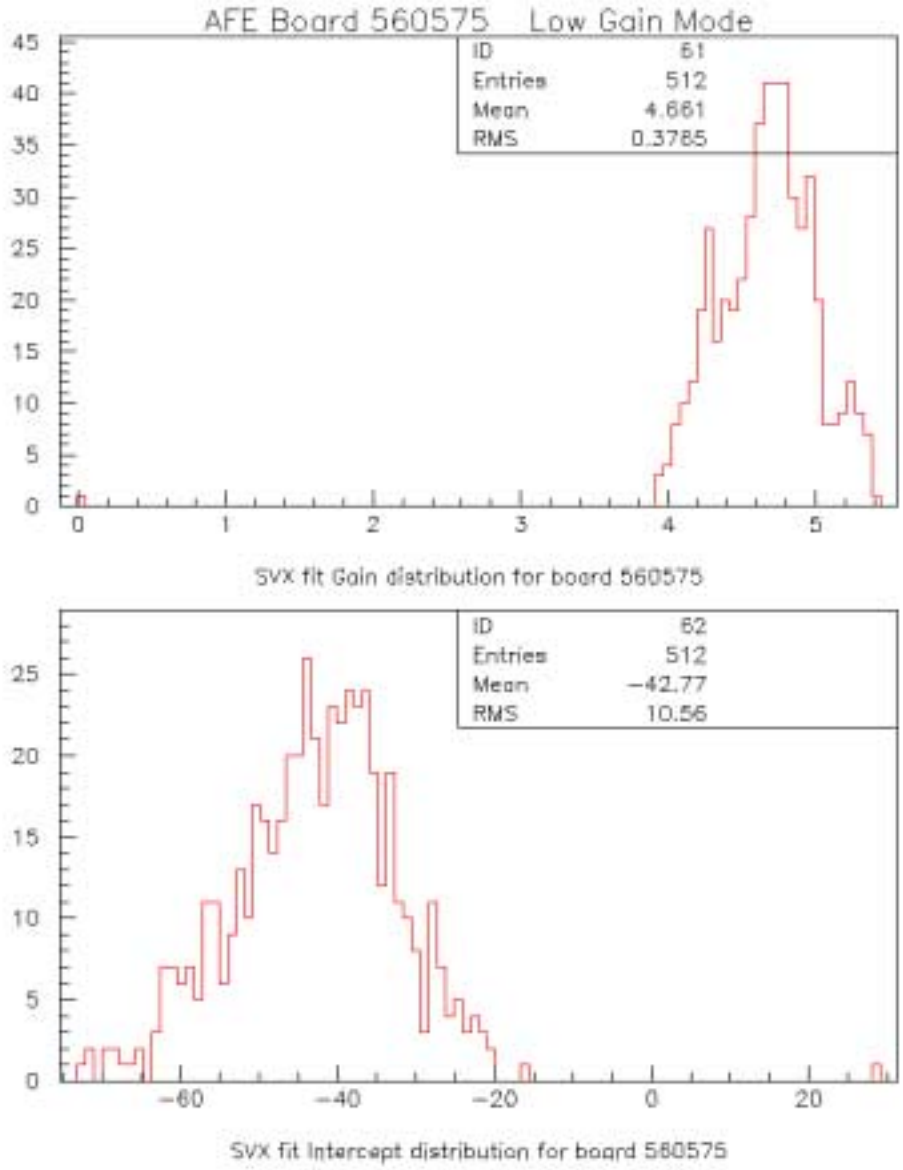


Fig. 8: Distributions of Fitted SVX gains and offsets displayed in Fig. 7.

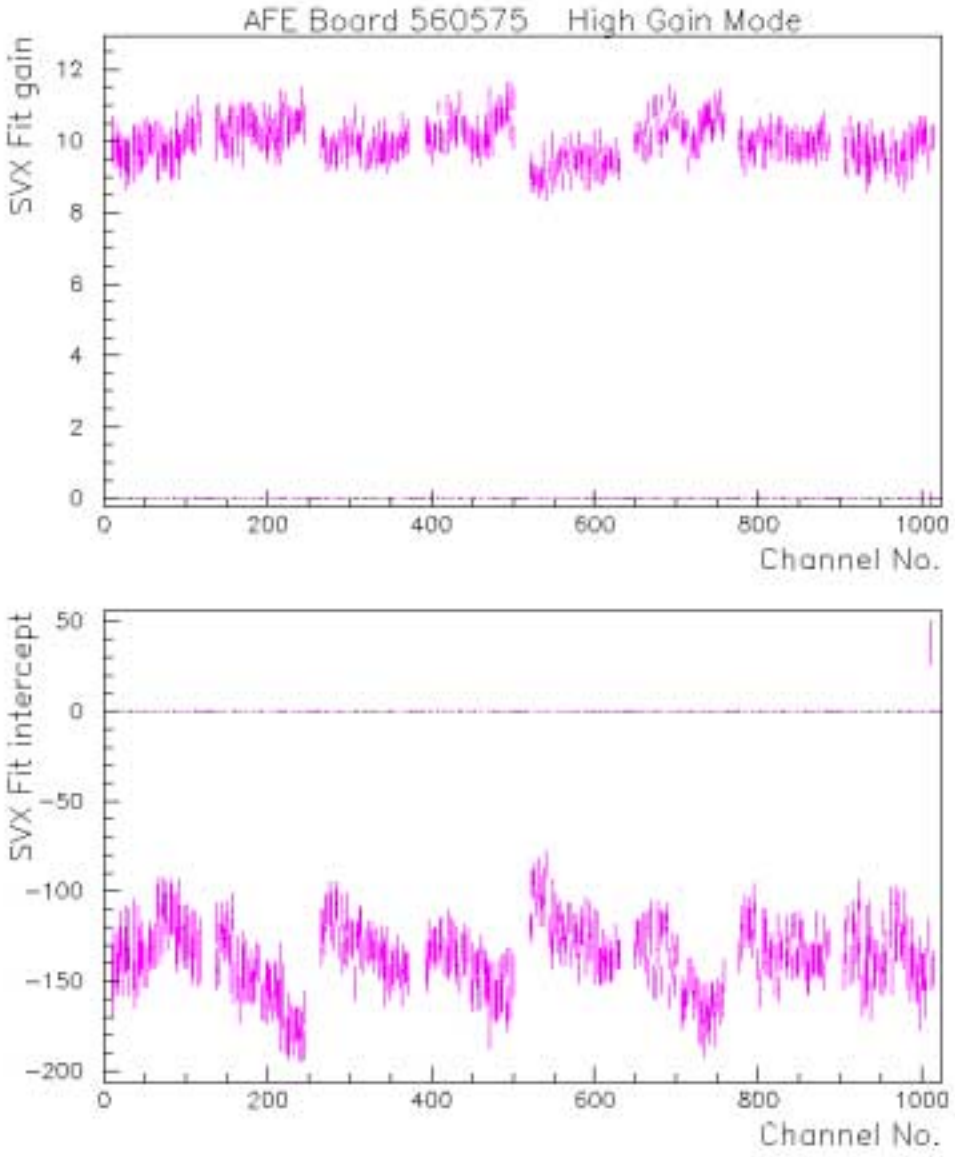


Fig. 9: Same as Fig. 7 in High Gain mode.

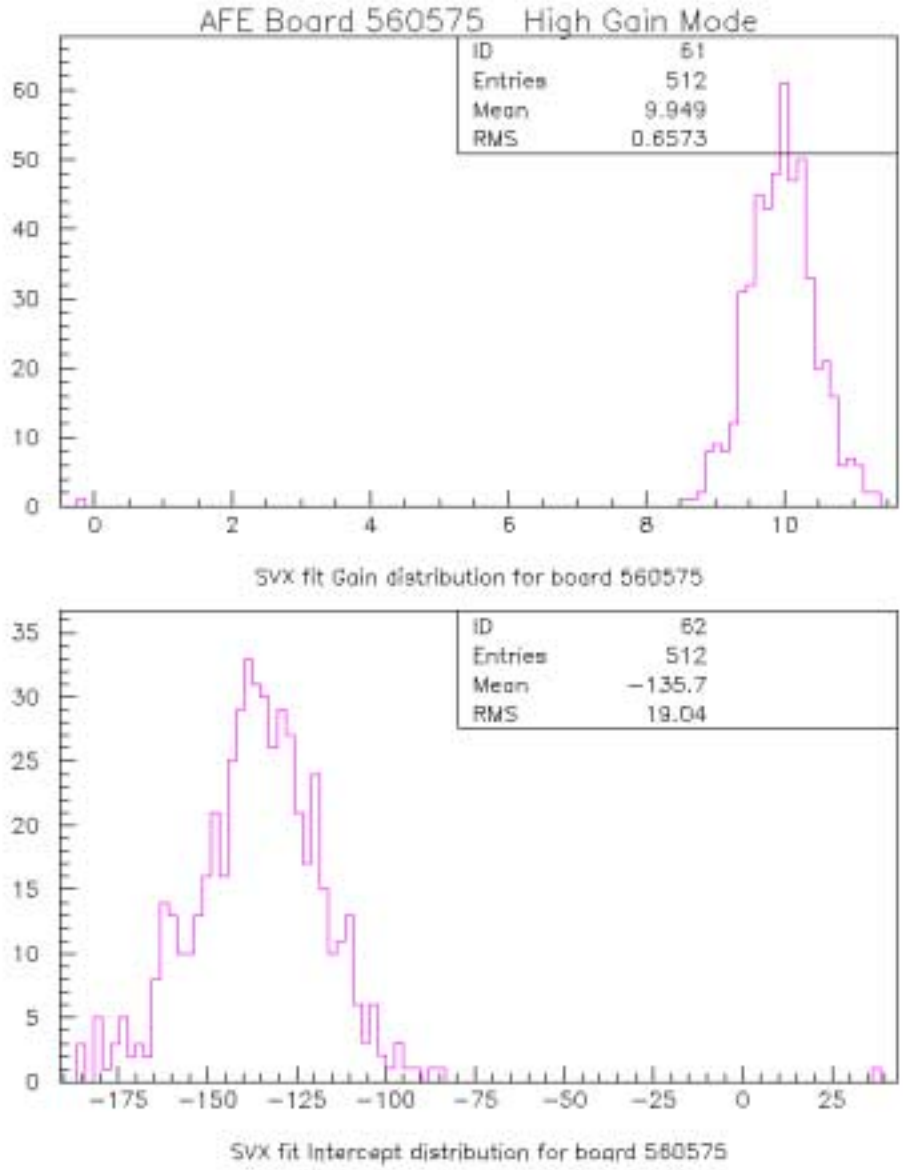


Fig. 10: Distributions of fitted SVX gains and offsets in High Gain mode.

Any channel that has its SVX gain less than 75% of the nominal (average gain for the board) is tagged as a bad channel.

5.5. Discriminator Threshold Scans

The test stand data also includes threshold voltage scans with different set amounts of charges injected (Q = 0, 20, 35, 50). For each amount of charge injected (and in case of no charge injection), the threshold voltage is varied and the digital output from the specific channels are read out. The output averaged over X events are plotted as the occupancy as a function of threshold voltage. These provide turn-on curves for each

channel and are shown in Figs. 11 and 12 (1 plot per SIFT) for an MCM for the cases Q = 0 and Q = 50 DAC units. (The turn-on value for each channel is taken to be the threshold voltage corresponding to 50% occupancy at a given charge.) We determine the turn-on width for each channel as the voltage difference between those corresponding to 10% occupancy and 90% occupancy.

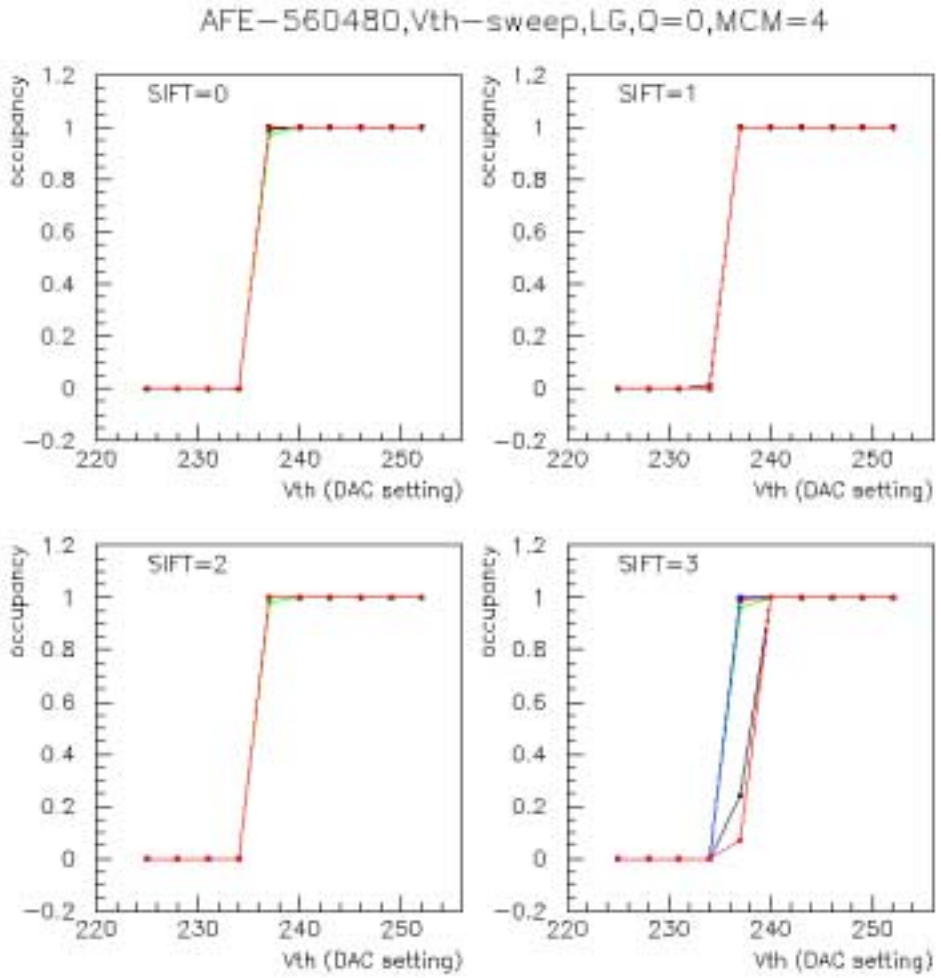


Fig. 11: Plots of average occupancy as a function of threshold voltage for each channel in a SIFT for MCM = 3 and AFE Board 560480 in the absence of charge injection. Most of the channels have overlapping discriminator turn-on.

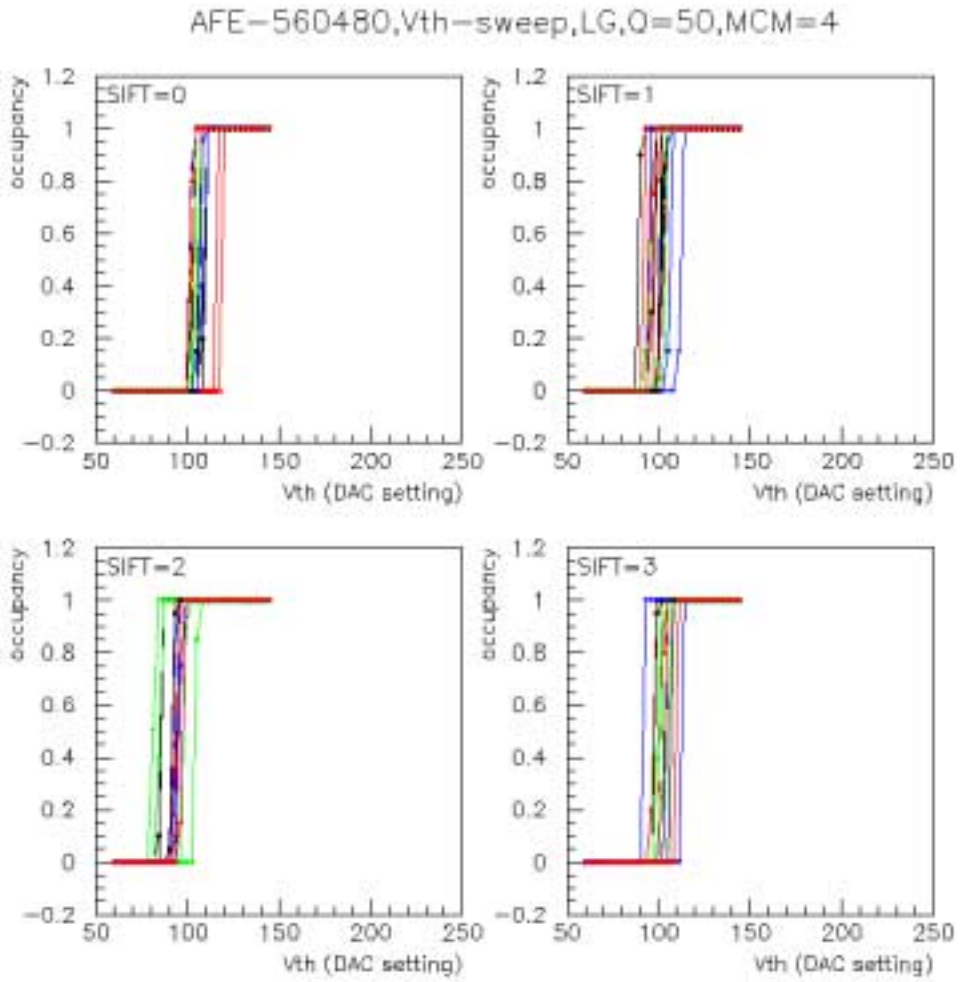


Fig. 12: Same as Fig. 11, but in the presence of injected charge Q = 50 DAC units

5.5.1. Discriminator Turn-On and SIFT Gains

The mid-point (50% average occupancy) of the turn-on curve for each injected charge Q is taken as the threshold voltage value (V_{th}). A linear fit is performed to this V_{th} as a function of Q to obtain the SIFT gain; the V_{th} values for the three Q values are shown in Fig. 13 for an AFE board. The discriminator/SIFT gains and offsets for all the channels are shown. The average SIFT gain for this board is –4.34. The distributions for gain and offsets are shown in Fig. 14.

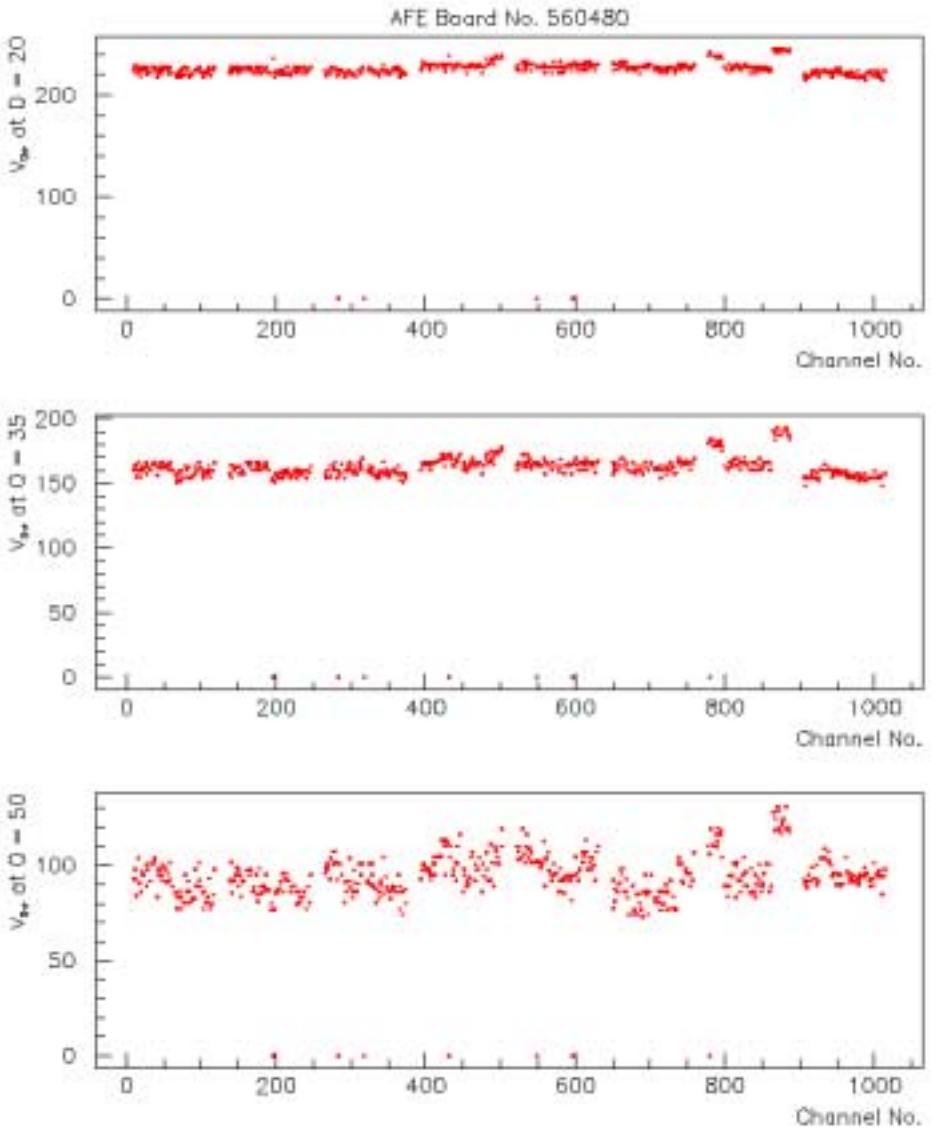


Fig. 13: The threshold voltages (calculated as V_{th} at 50% average occupancy) for each channel at Q = 20, 35 and 50 QDAC units for AFE board 560480.

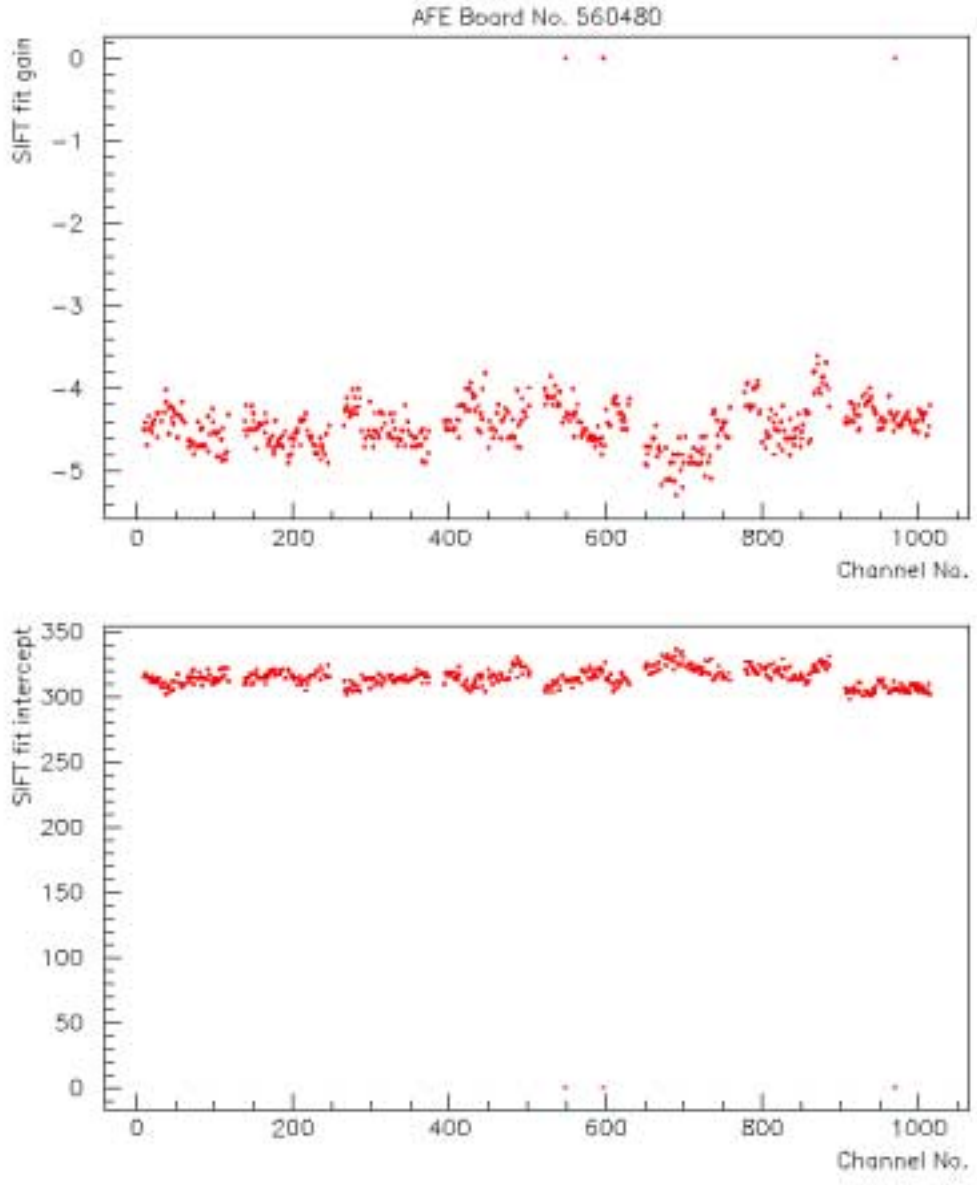


Fig. 14: SIFT gains and offsets for all channels using data from Fig. 13.

Again, as in the case of SVX gain, any channel that has a gain less than 75% in magnitude of the average SIFT gain for the board is tagged as a bad channel.

5.5.2. Turn-On Width

For each channel, using the threshold voltage scan data (see Figs. 11 and 12), we determine the discriminator turn-on width as the difference in V_{th} for average occupancies of 10% and 90%. They are typically 3-6 DAC counts.

5.6. Zero Suppression Threshold Studies

5.6.1. Pedestals from Phase-5 Tests

We studied the zero suppression threshold issues for 50 AFE boards as part of the Phase-5 analysis. The initial goal of this test was to find zero suppression thresholds for every SIFT/MCM allowing for certain occupancy and to determine the number of bad channels a board has for a chosen threshold. The number of bad channels would then be included in the total number of bad channels reported for the board, to be used to classify the board. Eventually, however, there were problems in determining and setting of appropriate V_{ref} voltages for different SIFT chips and also concerns that the behavior of the pedestals on the platform could be quite different than in Phase-5. So, we decided that it is not useful to include the bad channels from the Phase-5 zero suppression study in the total bad channel count for board certification. We, however, describe the study with Phase-5 data here.

5.6.1.1. Finding the Threshold

For each SIFT, the SVXmean (mean pedestal) values are used to define a rough zero suppression threshold. Since there are 4 SIFTs in each MCM and 8 MCMs on an AFE board each board gets 32 different thresholds.

In Fig. 15 the SVXmean values for MCM number 1 for board 560606 are shown.

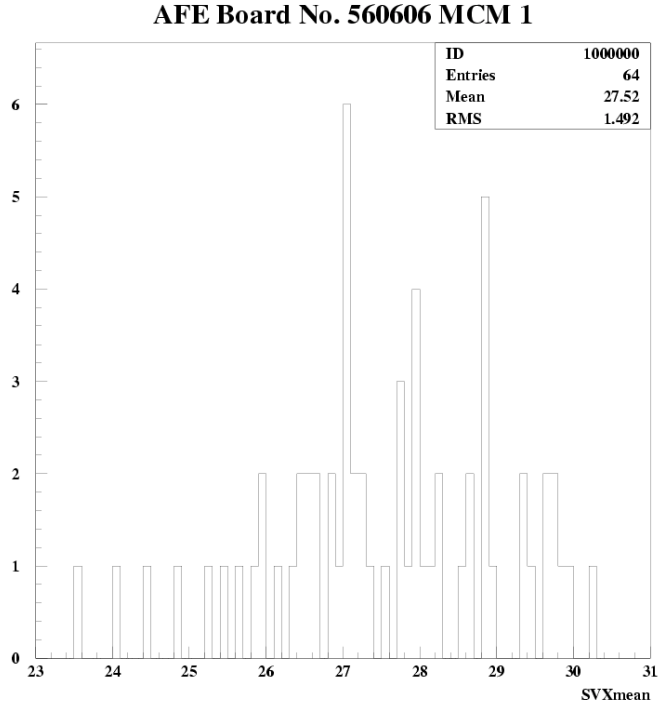


Fig. 15: SVXmean values for MCM1, AFE-board 560606

In the first iteration of the study a zero suppression threshold for each MCM was considered but because of the wide spread in SVXmean values the number of bad channels was too high. Therefore, subsequently, a threshold for each SIFT was considered. Fig. 16 shows the data for MCM 1 for each of the four SIFTs separately.

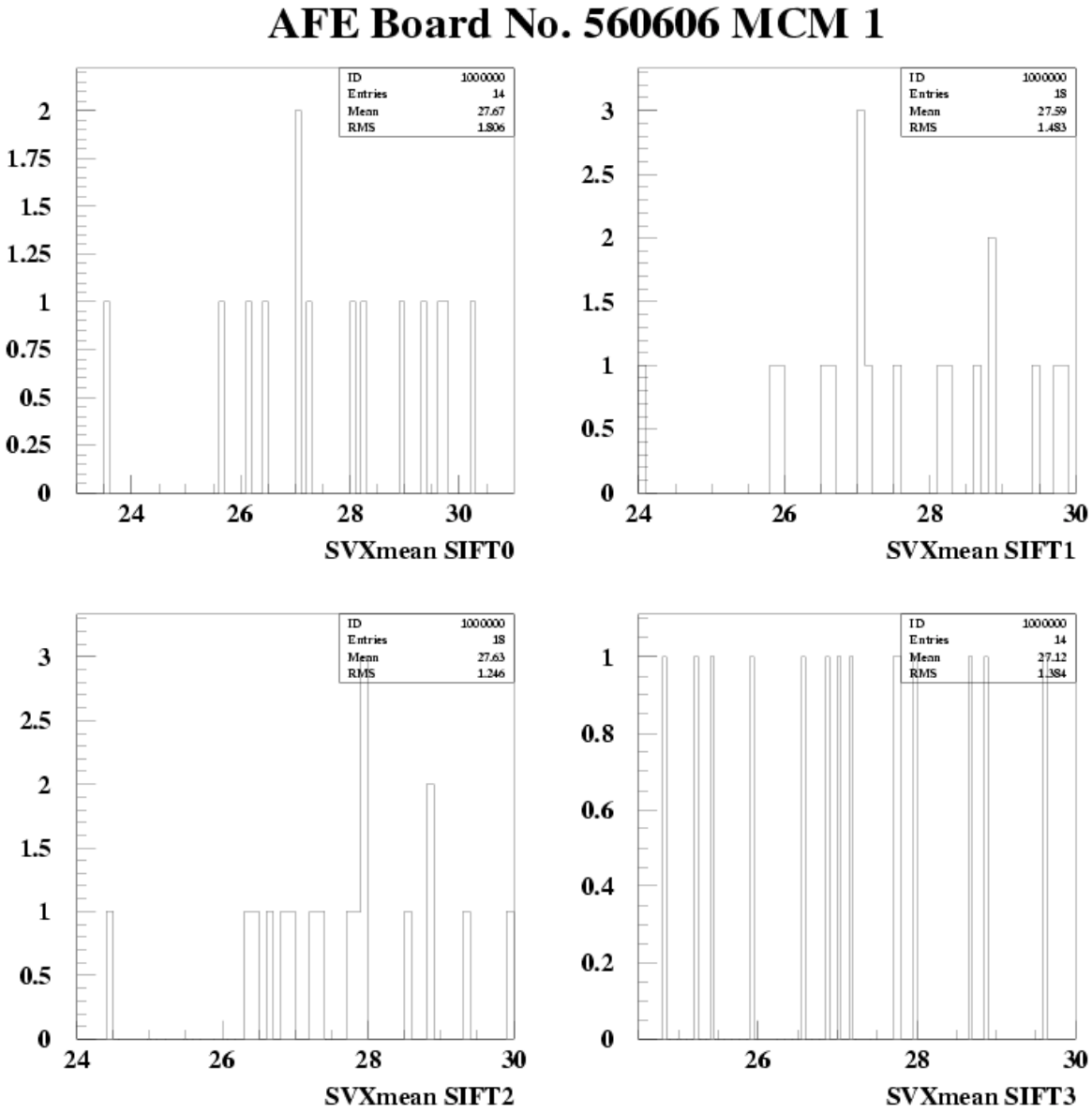


Fig. 16: SVXmean values for each SIFT of MCM1, AFE-board 560606

5.6.1.2. Strategy

To find a proper threshold the following strategy is used. First one determines the maximum pedestal mean for each SIFT, i.e. one looks for the last filled bin. To have a sensitivity for two photoelectrons, 14 ADC counts (because the tests were done in LG

mode) are subtracted from this maximum and channels which have SVXmean entries below that are identified and labeled as bad channels. If there are any bad channels found, a new zero suppression threshold was applied. To this purpose the last filled bin below the first threshold is taken as a new threshold (that is the channel with mean below the highest). Then 14 ADC counts are subtracted again and bad channels below this value are looked for. If there are any we look for a third threshold and if necessary for a fourth threshold as well. The search for bad channels is applied for all thresholds in the same way as described above.

As an illustration of this procedure Fig. 17 shows the SVXmean distribution for SIFT 1 of MCM2 and board 560568. The last filled bin and consequently the maximum pedestal has the SVXmean of 35.86. After subtraction of 14 ADC counts 5 bad channels are found for the given threshold (left of the arrow). If we apply the zero suppression threshold at the second maximum there are no bad channels left because of the big gap between the last but one and the last filled bin.

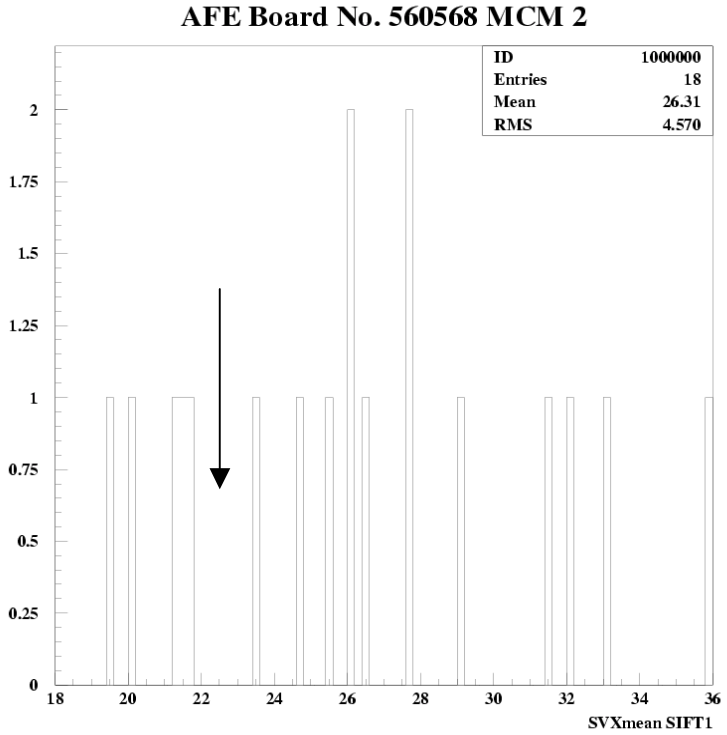


Fig. 17: SVXmean distribution for SIFT1 of MCM2 of board 560568

For boards that have a big number of bad channels the SVXmean values are clustered in some regions resulting in a lot of gaps dispersed over the whole SVXmean distribution.

5.6.1.3. Results

36 boards out of 50 had pedestal widths below 14 counts for all SIFTs so they had 0 bad channels with zero occupancy above the threshold. 14 boards out of 50 had bad channels by applying the threshold below the maximum pedestal. By applying the threshold below the second maximum only 10 boards with bad channels are left. It is possible to reduce this number to 7 boards if the threshold is set below the third maximum. Table 1 shows it is not possible to reduce this number again by applying a new threshold. Table 1 summarizes the number of bad channels for these 14 boards.

Channels about threshold	***1***	***2***	***3***	***4***
Board ID	***Number of bad channels***			
560 456	25	9	5	4
560 520	2	1	1	1
560 568	64	26	22	22
560 593	8	6	5	4
560 633	1	1	1	1
560 634	71	42	32	18
560 646	32	17	13	6
560 473	3	1		
560 512	5	2		
560 628	1	1		
560 502	7			
560 540	1			
560 555	8			
560 699	1			

Table.1: Number of bad channels as a function of number of channels above threshold.

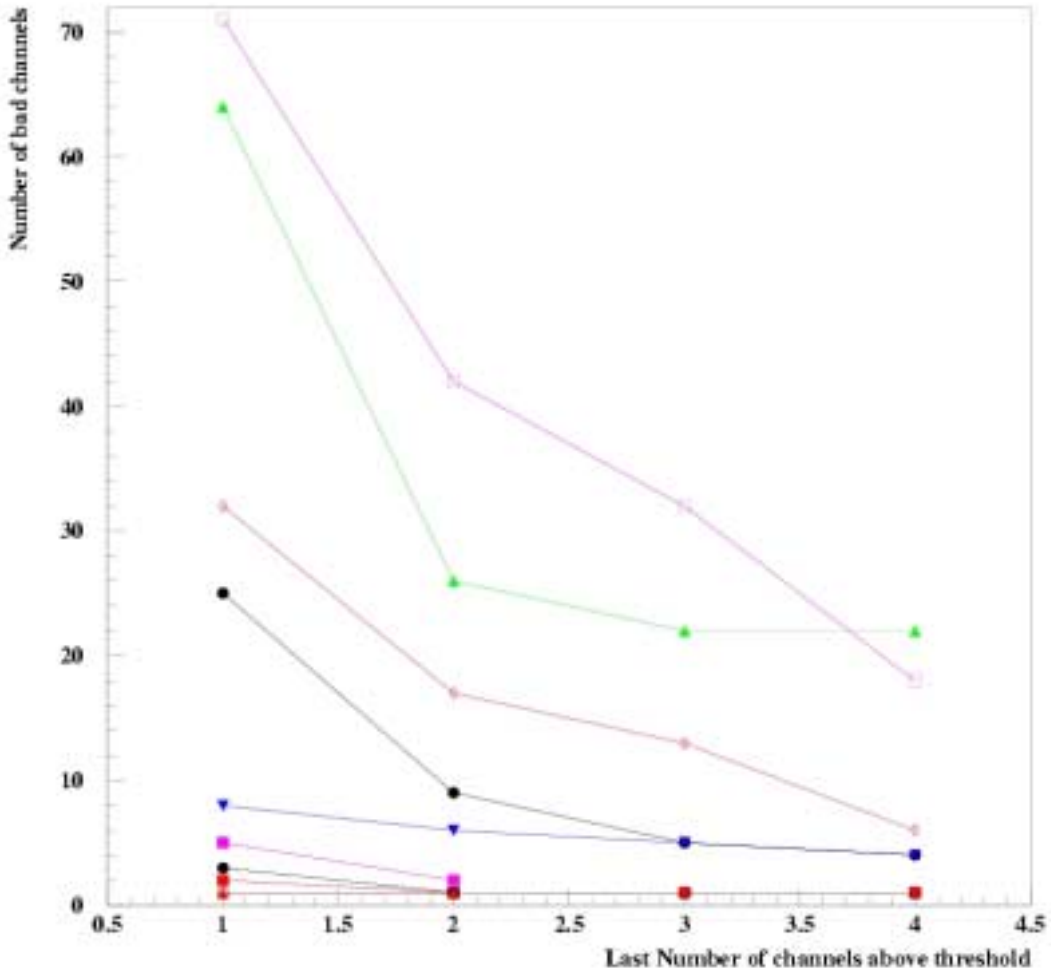


Fig. 18: Number of channels above threshold.

5.6.2. Pedestals from Platform Tests

We also analyzed pedestal data recorded for 10 AFE boards on the platform. These 10 boards have board-numbers:

560464, 560453, 560519, 560498, 560525, 560558, 560561, 560542, 560562, 560489

The distribution of pedestals (calculated in p.e. units and mean subtracted) for channels in each SVX of the board 560464 is displayed in Fig. 19. In Fig. 20(top), the pedestals of all channels from all 10 boards are shown. Fig. 20(bottom) shows the distribution of the RMS of the pedestal reading for each channel in all 10 boards. Since the platform data was taken in the High Gain mode, we assume 1 photoelectron (p.e.) = 15 ADC counts.

We then calculate the probability for pedestal above a given cut. The probabilities for each SVX of one board are shown in Fig. 21 and for all 10 boards are shown in Fig. 22. If we request 3% occupancy, for example, the cut will be over 2 p.e.. In Fig. 23 we use the mean of each SVX as the zero point to calculate the probability of

the pedestals over a given cut of all 10 boards and the cut will be 1.2 p.e. for 3% occupancy. In Fig. 24, we use the mean of each SIFT as the zero point to calculate the probability of the hits over a given cut of all 10 boards and the cut will be 1.0 p.e. for 3% occupancy.

So, the best sensitivity to signal can be achieved by setting the zero suppression threshold separately for each SIFT (as anticipated). In principle the V_{ref} on these boards are set to bring pedestal means of all the 4 SIFTs within a small range.

6. Board Certification Issues

6.1. Definition of a Bad Channel

A channel is defined as bad using the following criteria:

1. **SVX and SIFT gain:** A channel is flagged as bad if its SVX or SIFT gain is < 75% of the nominal SVX gain or SIFT gain, respectively. Nominal gain is taken as average gain for the board.
2. **SVX pedestal sigmas:** A channel is flagged as bad if its SVX pedestal sigma is > 1 p.e. (7 ADC counts).
3. **Discriminator turn-on:** A channel is flagged as bad if the turn-on defined as the width in DAC counts for 0 to 90% occupancy is greater than 2 p.e. (14 DAC counts assuming SVX and SIFT gain are about equal)
4. **SVX zero suppression:** A SIFT is flagged as bad if the pedestal mean distribution for the 14 or 18 channels in the SIFT has a full width greater than 2 p.e. (14 ADC counts). The bad channels are those channels whose pedestal mean is more than 14 ADC counts below the maximum pedestal mean.

Even though, we performed some simple and crude studies of zero suppression as explained in section 5.6, we did not use the fourth criterion (the zero suppression criteria) for grading and selecting boards for commissioning. More careful and sophisticated studies of pedestals, their variations and occupancies are needed, post-installation, to establish appropriate zero-suppression thresholds and to tag bad channels.

6.2. Criteria for Grading AFE Boards

For commissioning the AFE boards, they were graded based on the number of bad channels that were found in the offline analysis of the Phase-5 data and a few other loose parsing criteria. The boards were rejected if the V_{ref} scans showed a spread wider than 1 p.e. for channels belonging to a SIFT.

The classifications were then performed as follows:

Class	Criteria
A	$N_{bad} < 8$ channels, Pass LVDS, Bias tests
B	$N_{bad} < 20$ channels, Not A.
C	$N_{bad} < 64$ channels

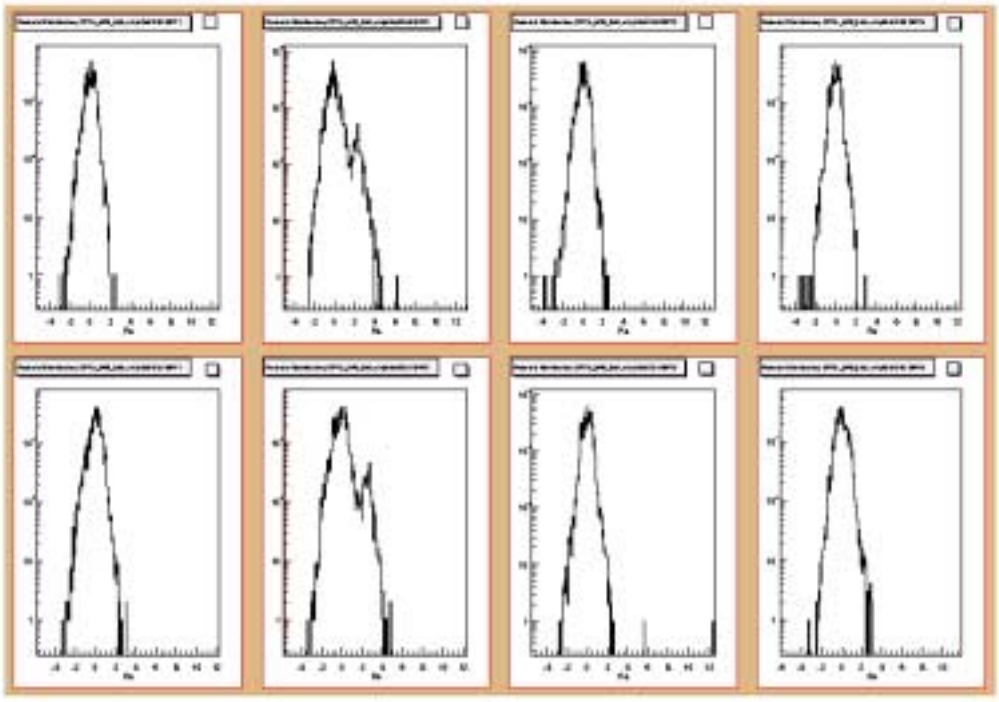


Fig. 19: Pedestal distributions in p.e. units (mean-subtracted) for channels in each MCM for board 560464.

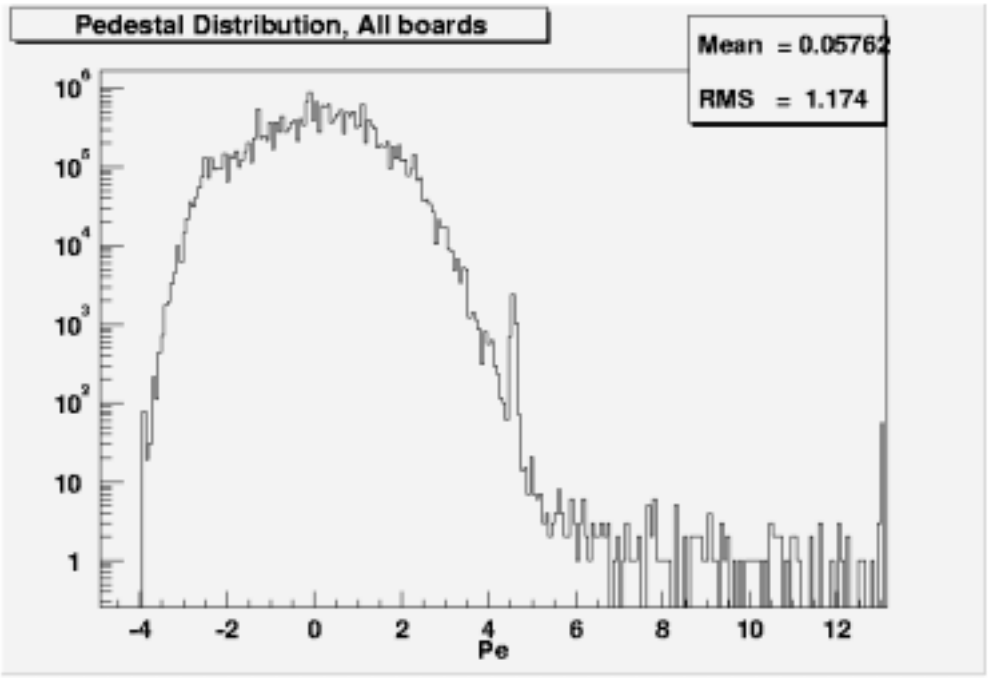
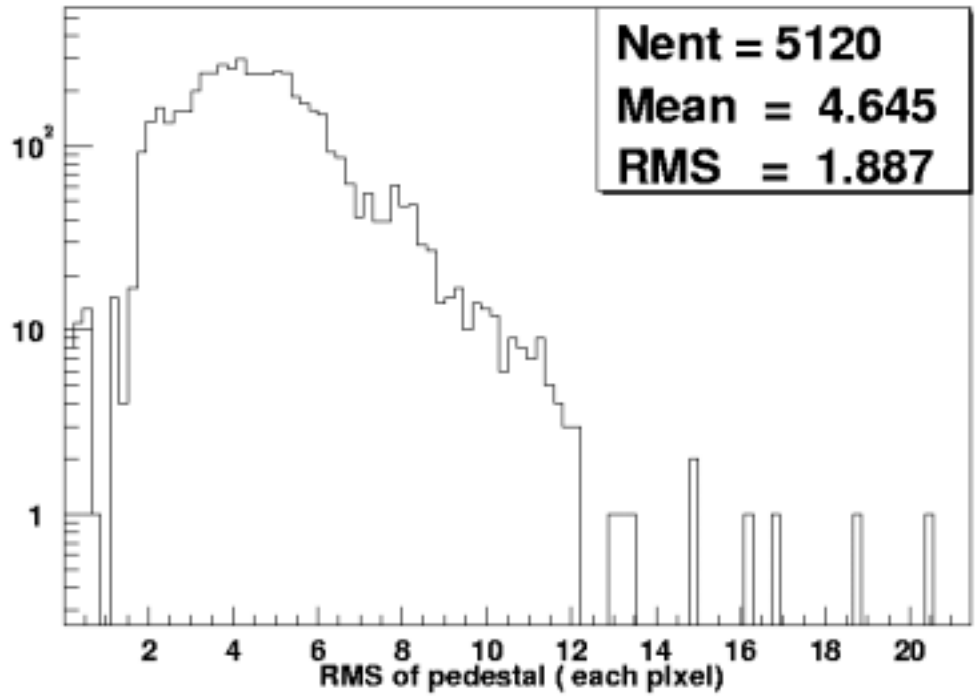


Fig. 20: **(Top)** Pedestals of all channels for 10 boards listed in section 5.6.2. **(Bottom)** RMS of pedestals for all channels for the 10 boards.



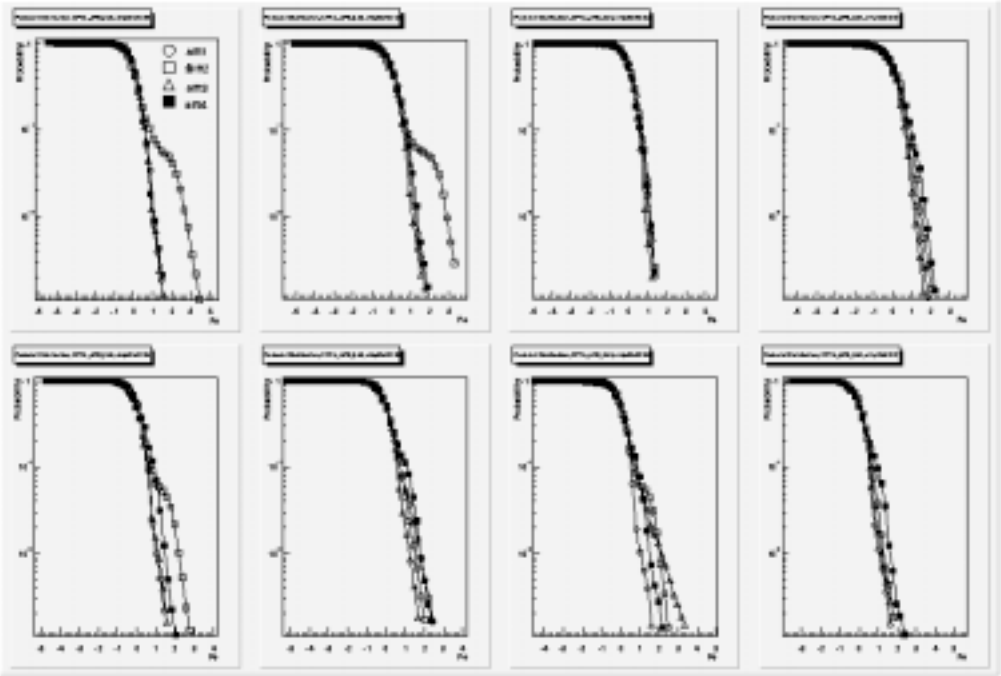


Fig. 21: Probability for pedestals above a given threshold for each SVX in a board. Separate curves are shown for each SIFT.

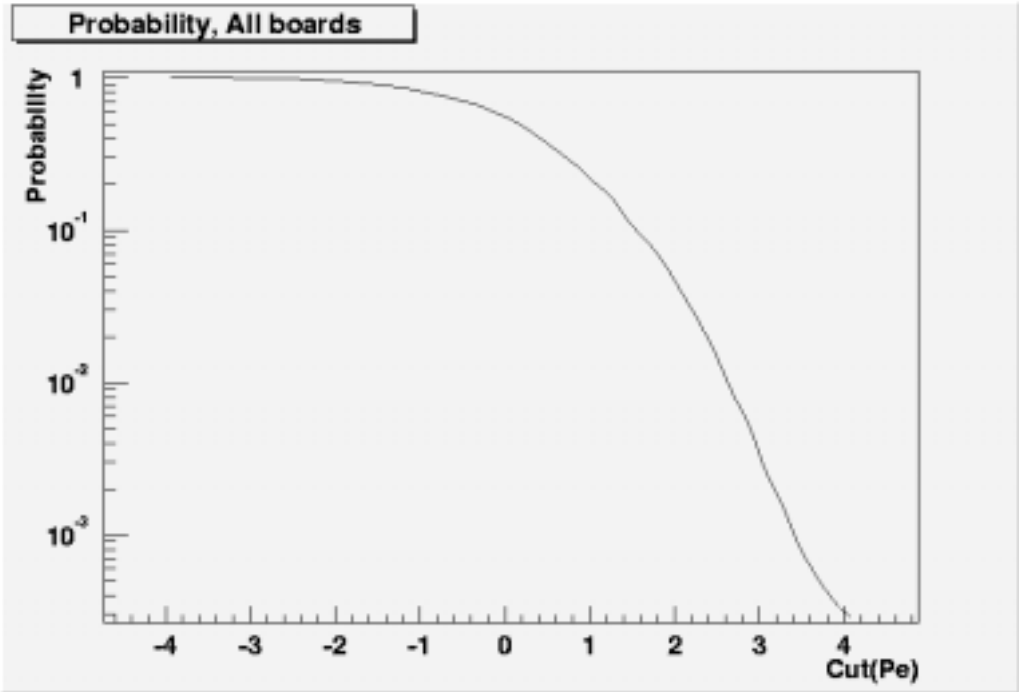


Fig. 22: Probability for pedestals above cut containing all boards.

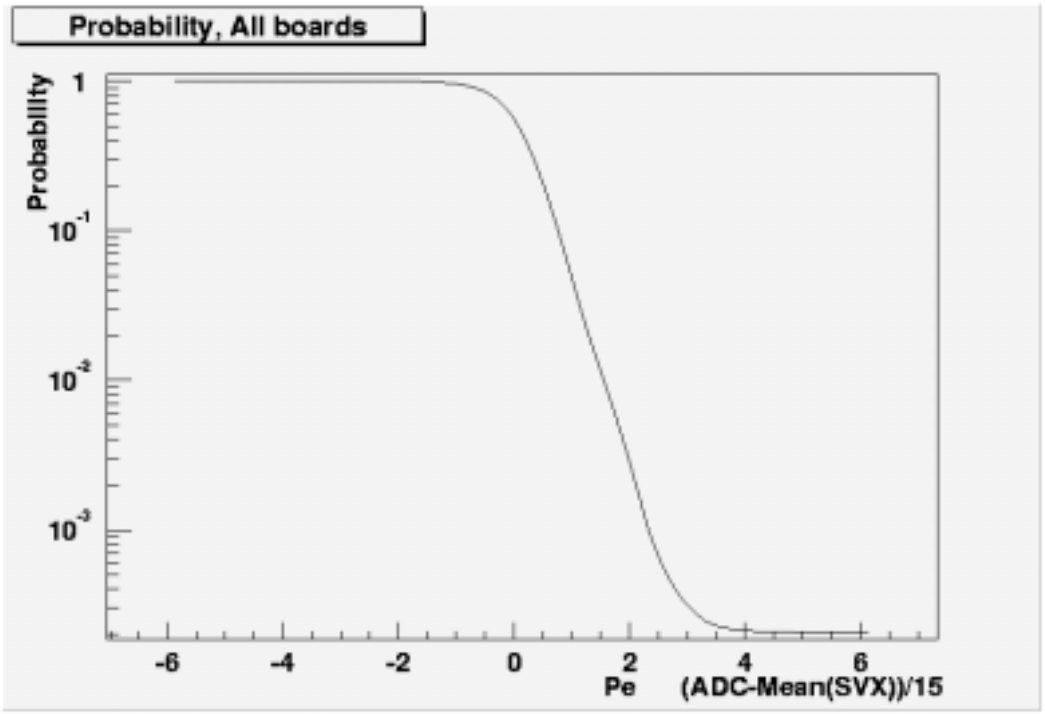


Fig. 23: Probability as in Fig. 22 but calculated after subtracting each SVX mean.

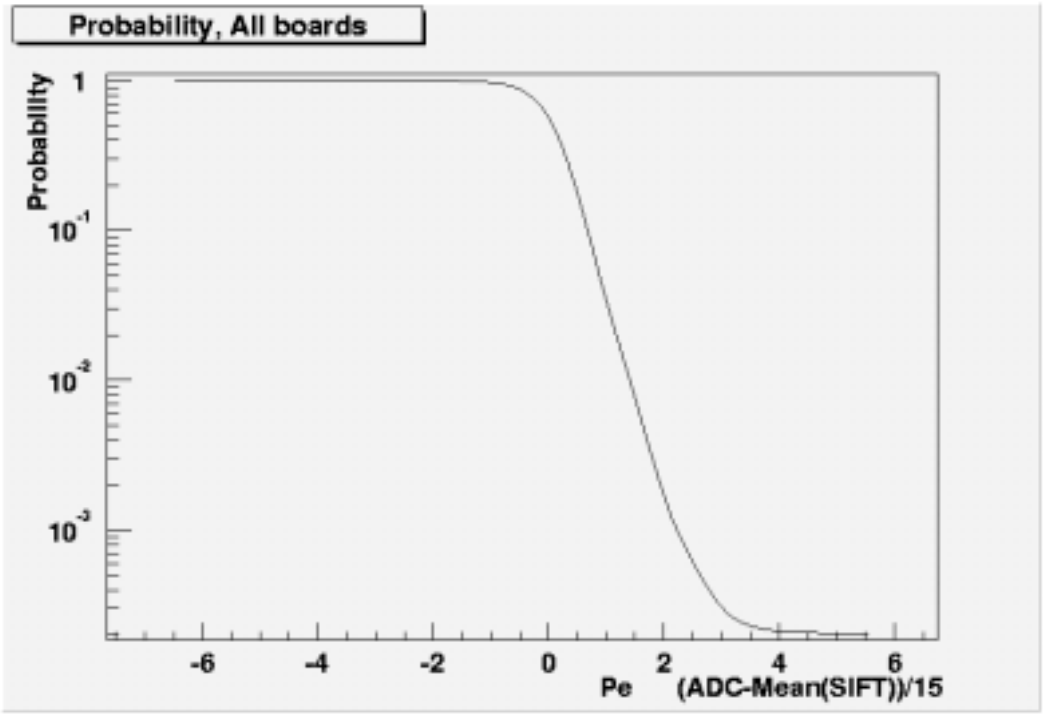


Fig. 24: Same as Fig. 23 but calculated after subtracting SIFT mean.

7. Summary

Here, we show some results of the offline analysis of the data from recent test data. Figs. 25 through 35 show various results and typical distribution of pedestals, SVX and SIFT gains, offsets, turn-on widths, etc. for a CFT/CPS board which instruments CFT channels with outer 4 MCMs and CPS channels with inner 4 MCMs.

To get a global perspective of all the AFE boards, we show plots of interesting quantities for all boards using latest test data for each board. First of all, we show the distributions of bad channels for all boards in Fig. 36. The installed boards have bad channels < 20 and mainly fall into the category of A or B class boards. Quite a bit of repair work was done to replace/repair SIFTs and/or MCMs to reduce the number of bad channels.

The pedestal mean and pedestal sigma distributions are shown in Fig. 37. The distributions of all SVX gains and SIFT gains are shown in Figs. 38 and 39.

The latest results of the Phase-5 data analysis for all the 198 AFE boards are stored in the form of tables and plots (such as examples shown in this note) in the cvs repository and can be accessed at
http://www-d0.fnal.gov/d0dist/dist/packages/afe_phase5/.

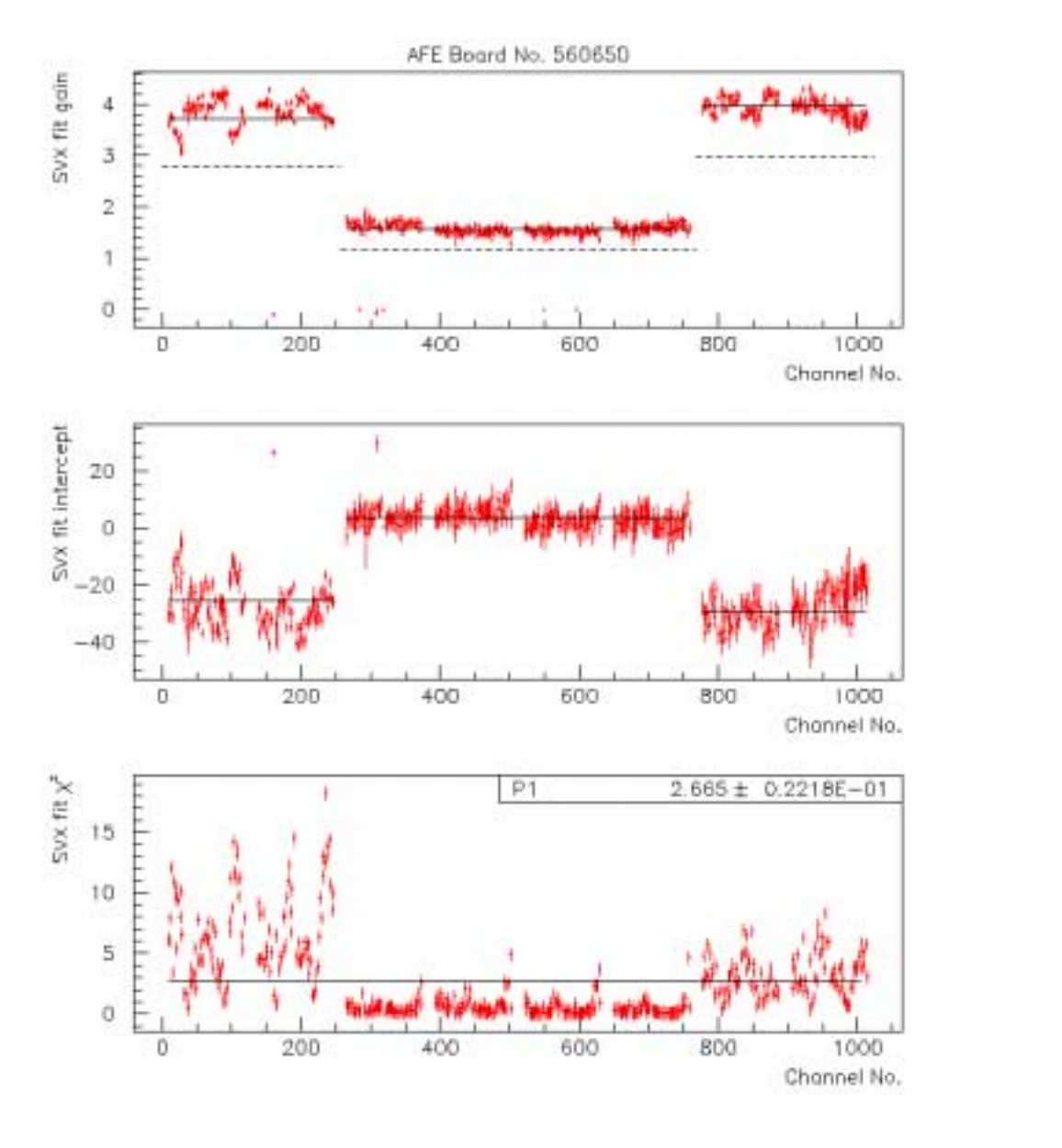


Fig. 25: Results from fits to SVX gain for a CFT/CPS board. The inner four MCMs are used for CPS and have gains smaller by approximately a factor of 2.

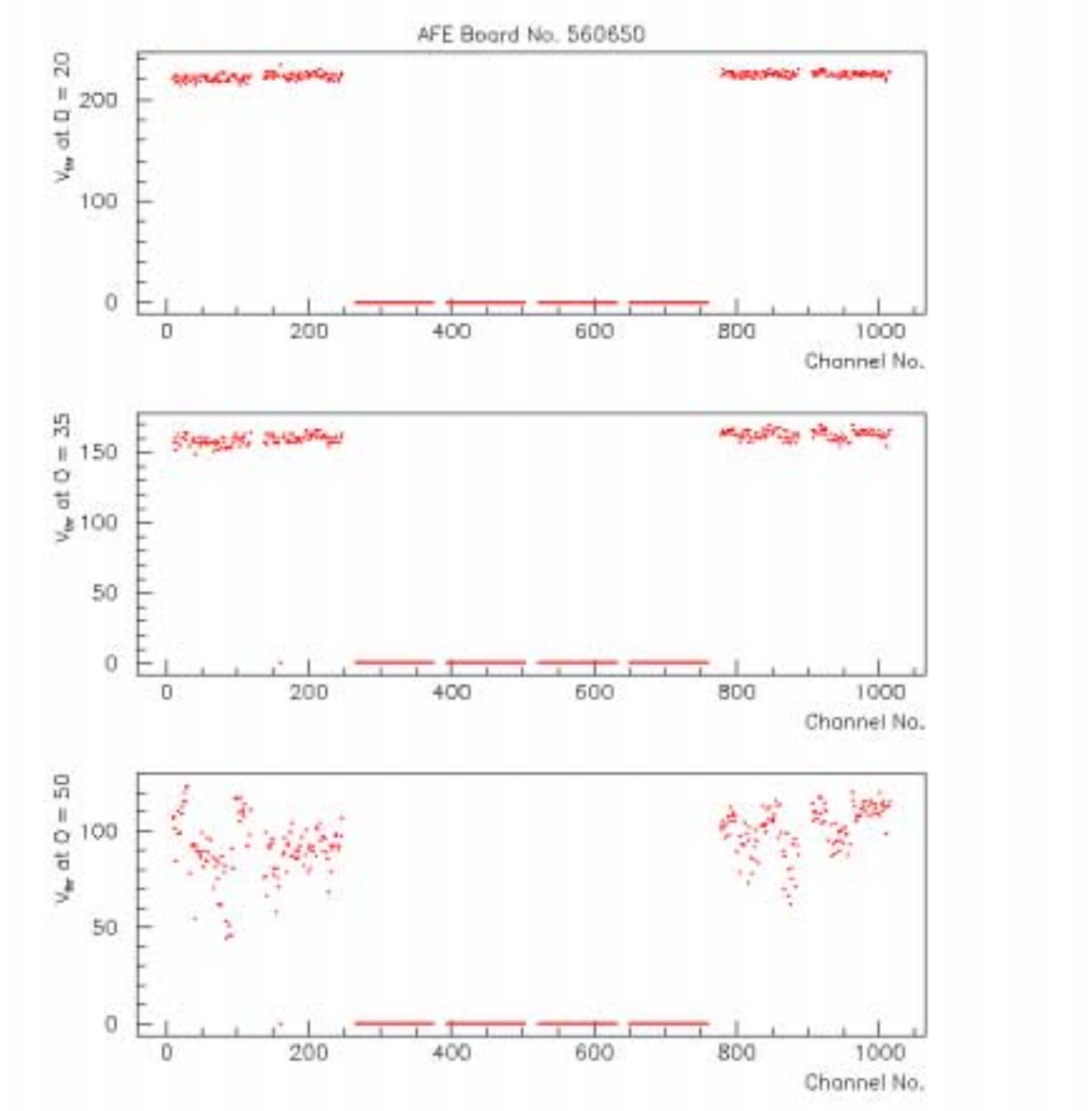


Fig. 26: Threshold voltage values (at 50% occupancy) for CFT channels at Q = 20, 35, 50 QDAC units (Ignore inner MCMs)

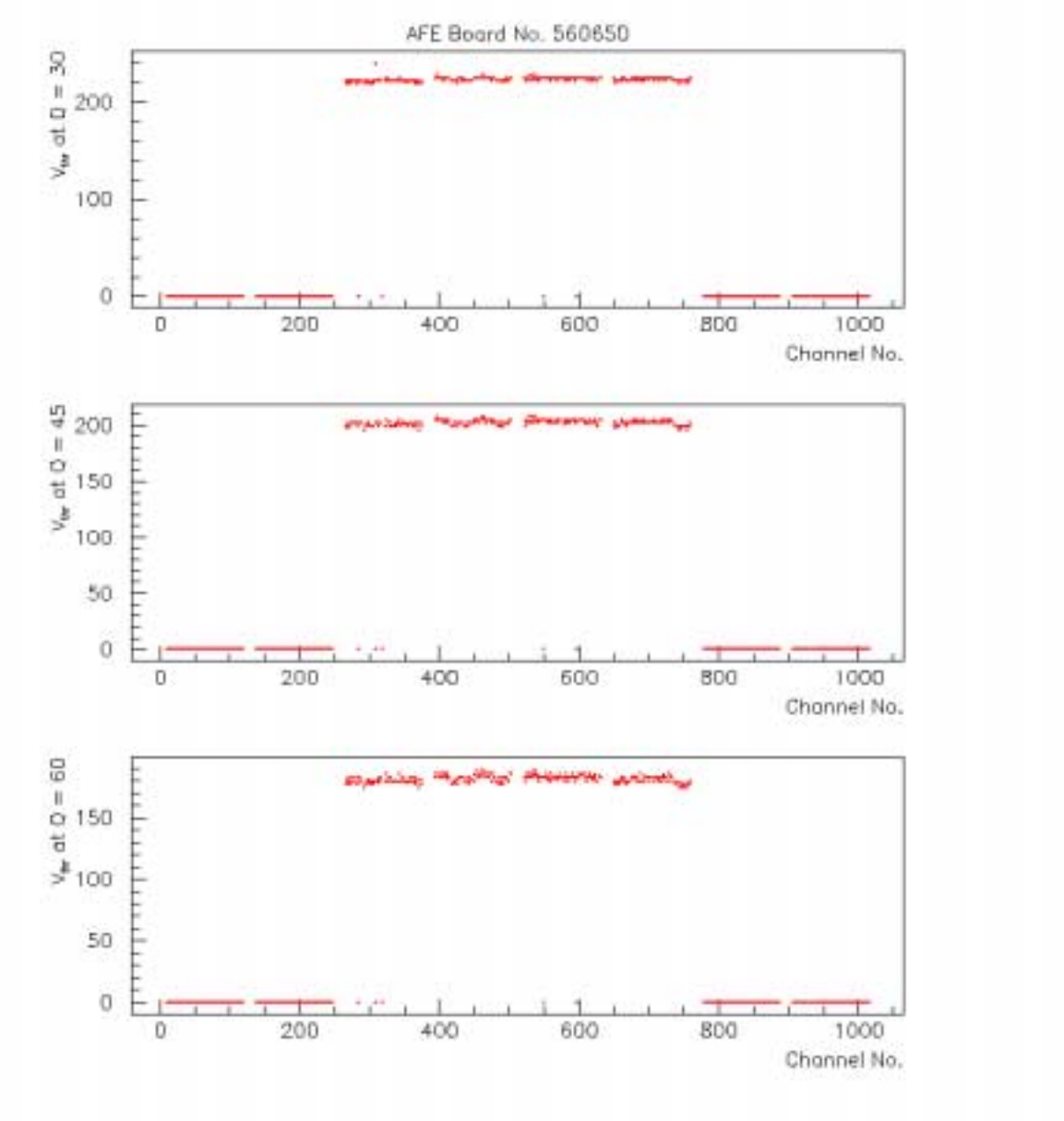


Fig. 27: Same as Fig. 26 for CPS channels (ignore outer MCMs)

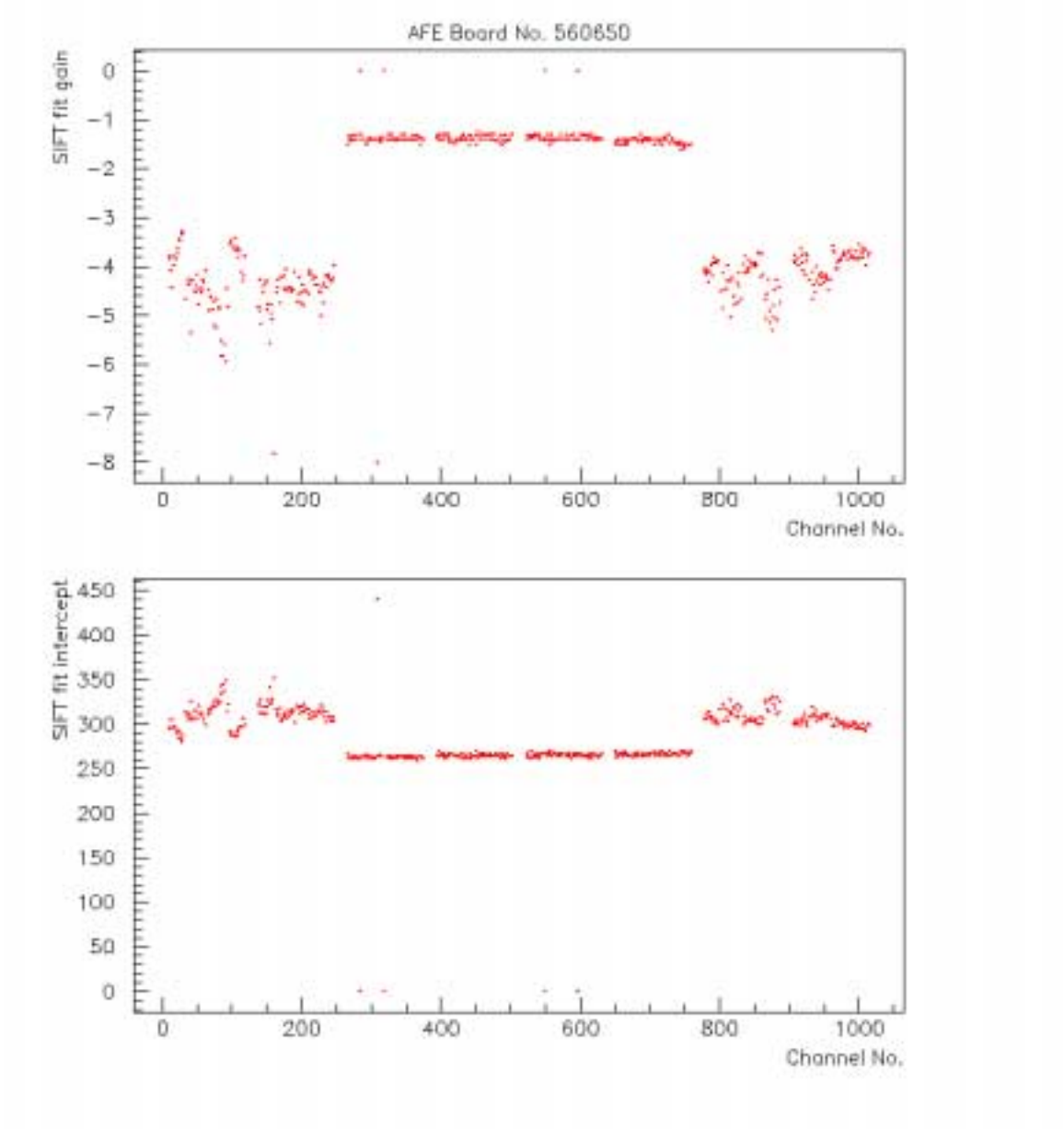


Fig. 28: SIFT gains and offsets obtained from linear fits to data from Figs. 26 and 27 for CFT and CPS channels respectively.

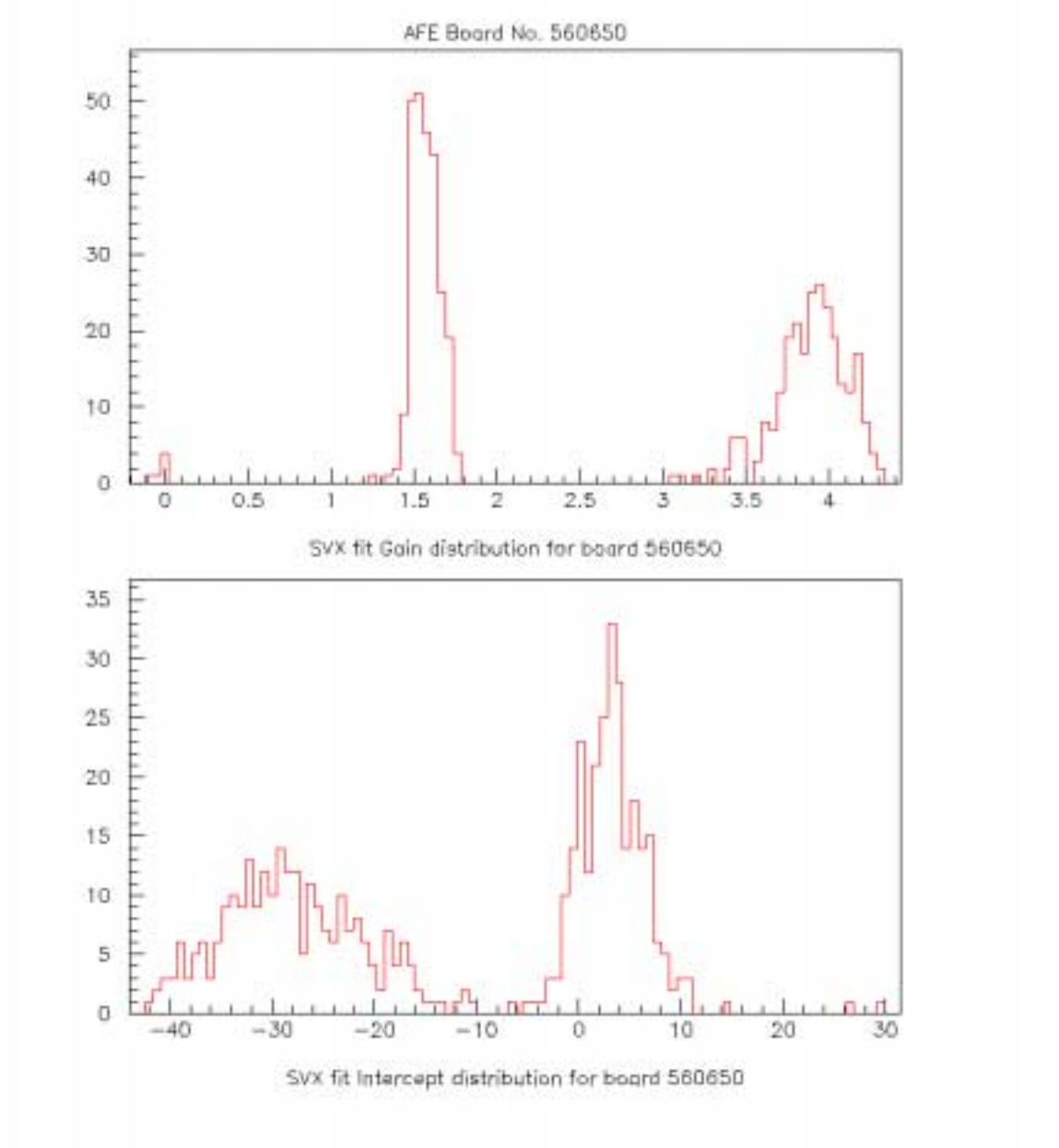


Fig. 29: Distribution of SVX fit gains and offsets.

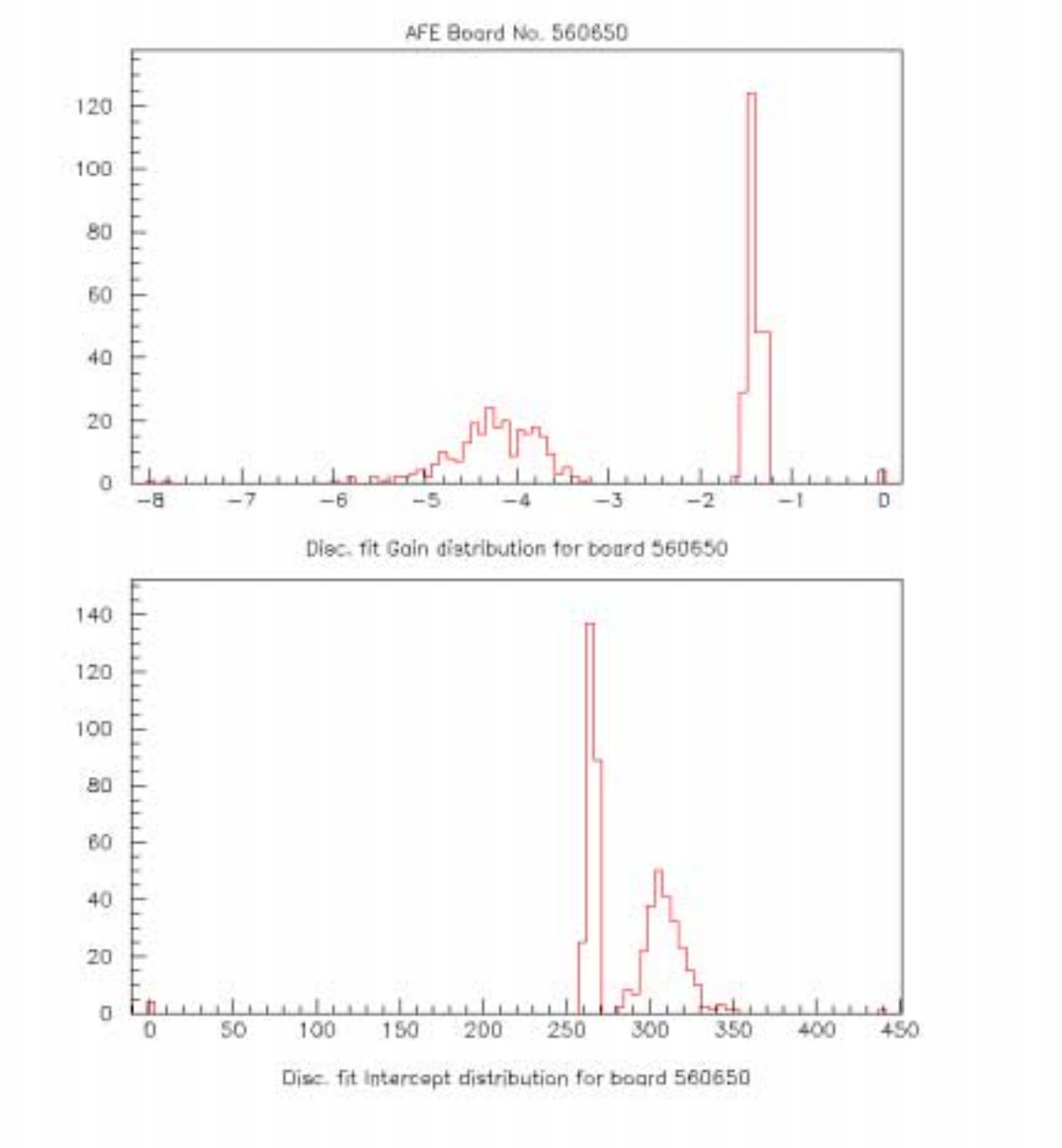


Fig. 30: Distributions of SIFT fit gains and offsets.

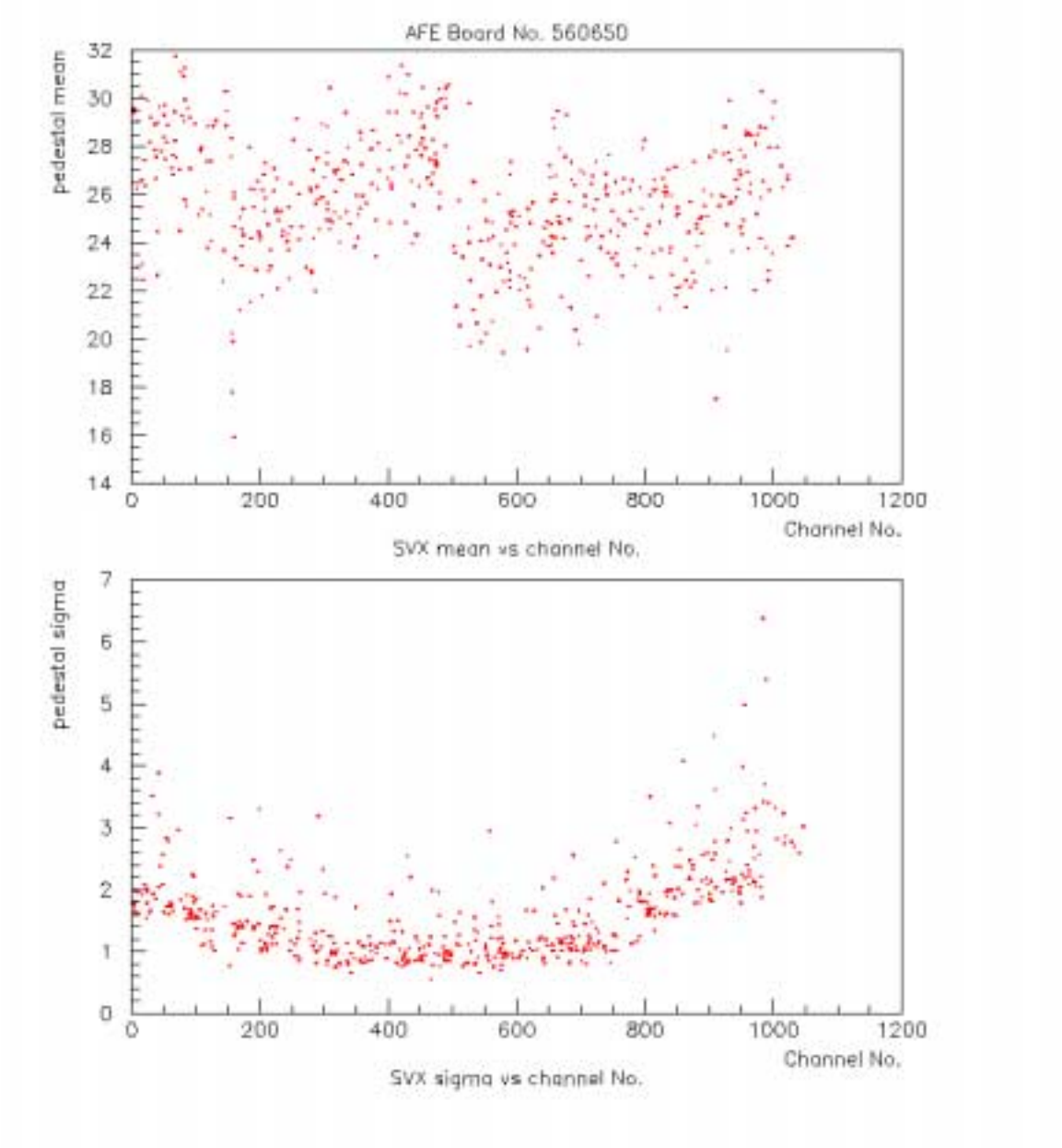


Fig. 31: Pedestal means and sigmas for all channels for board 560650.

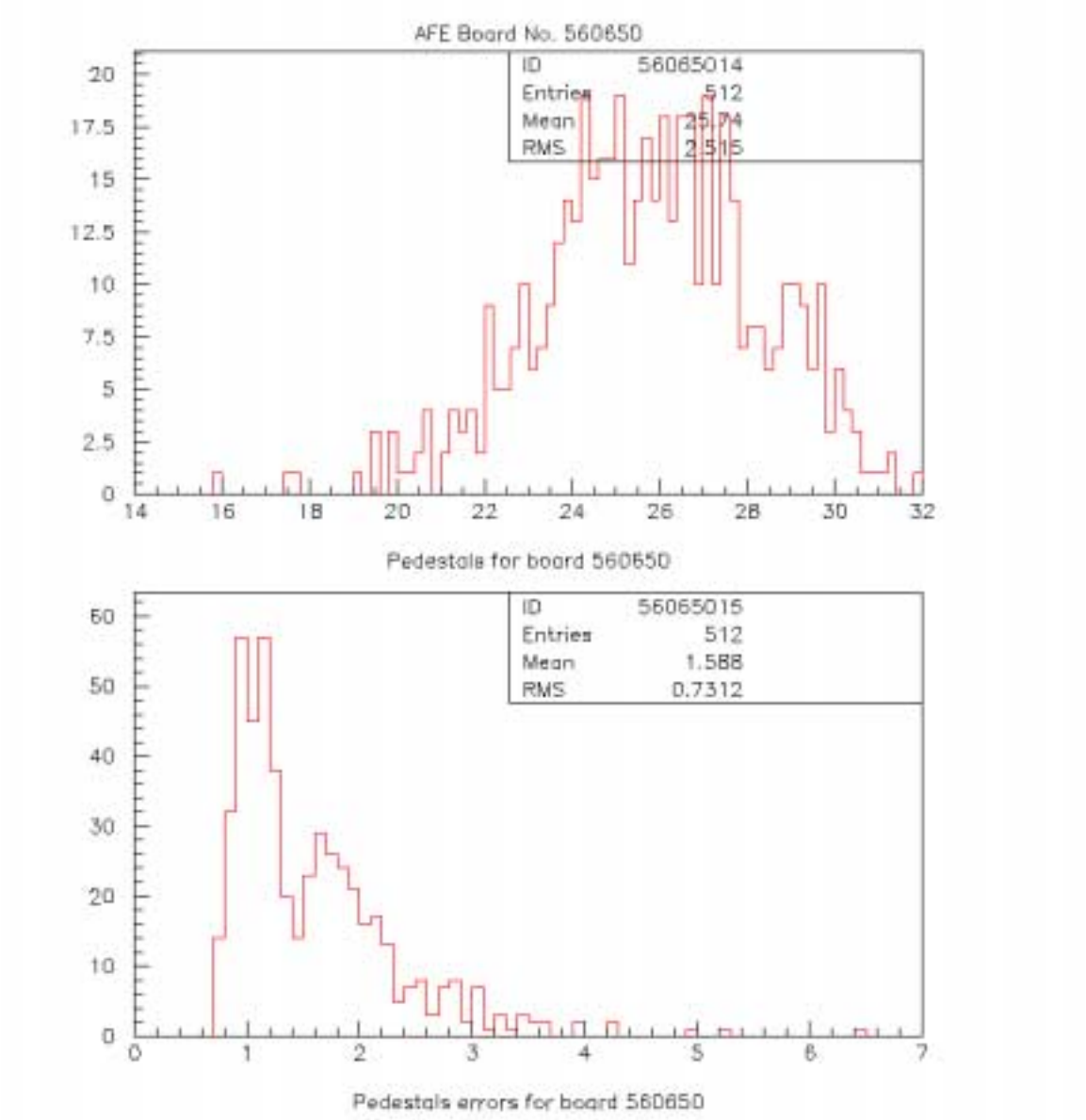


Fig. 32: Distributions of pedestals and pedestal errors for board 560650.

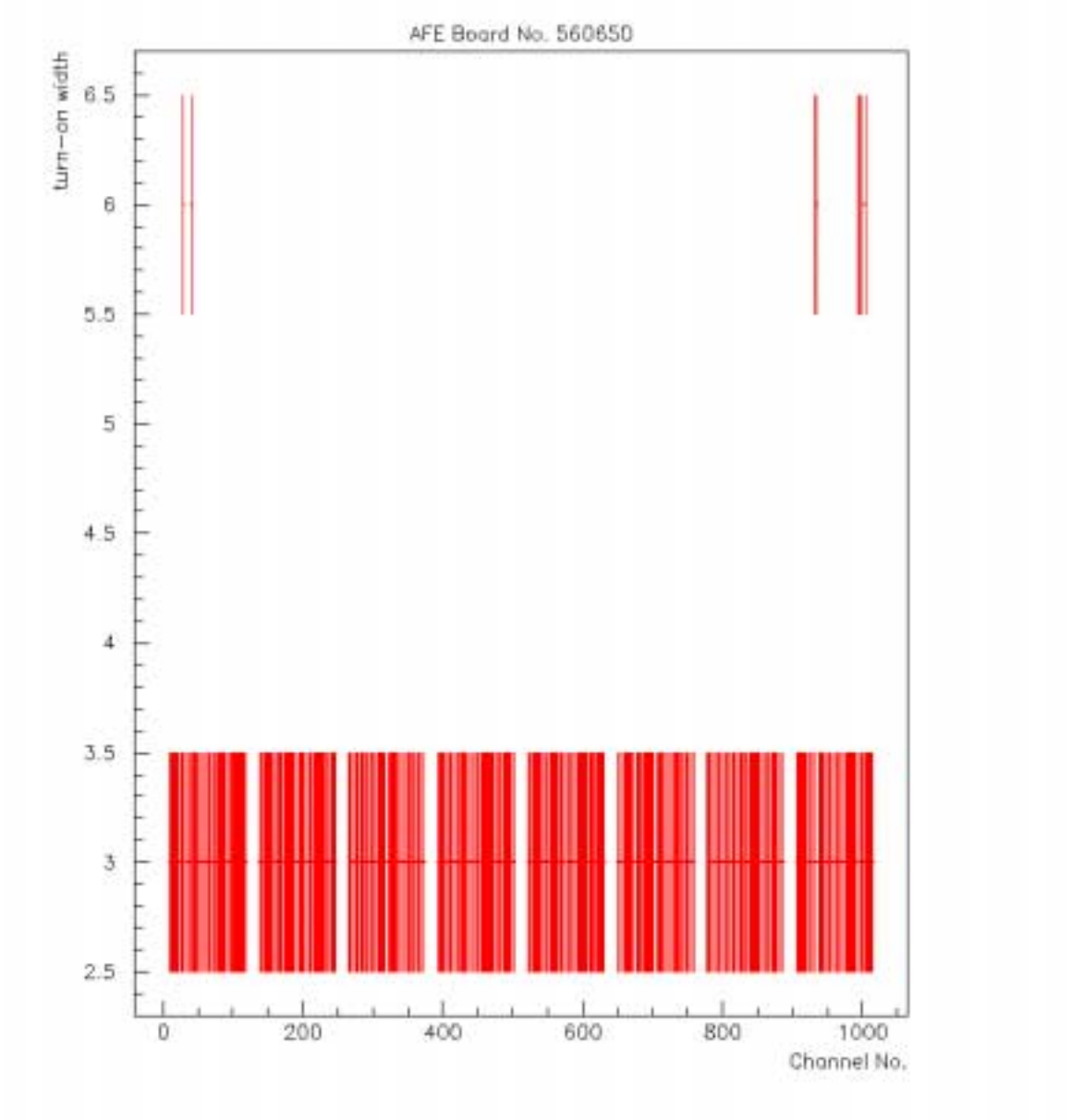


Fig. 33: Discriminator turn-on width in DAC units for all active channels in AFE board 560650.

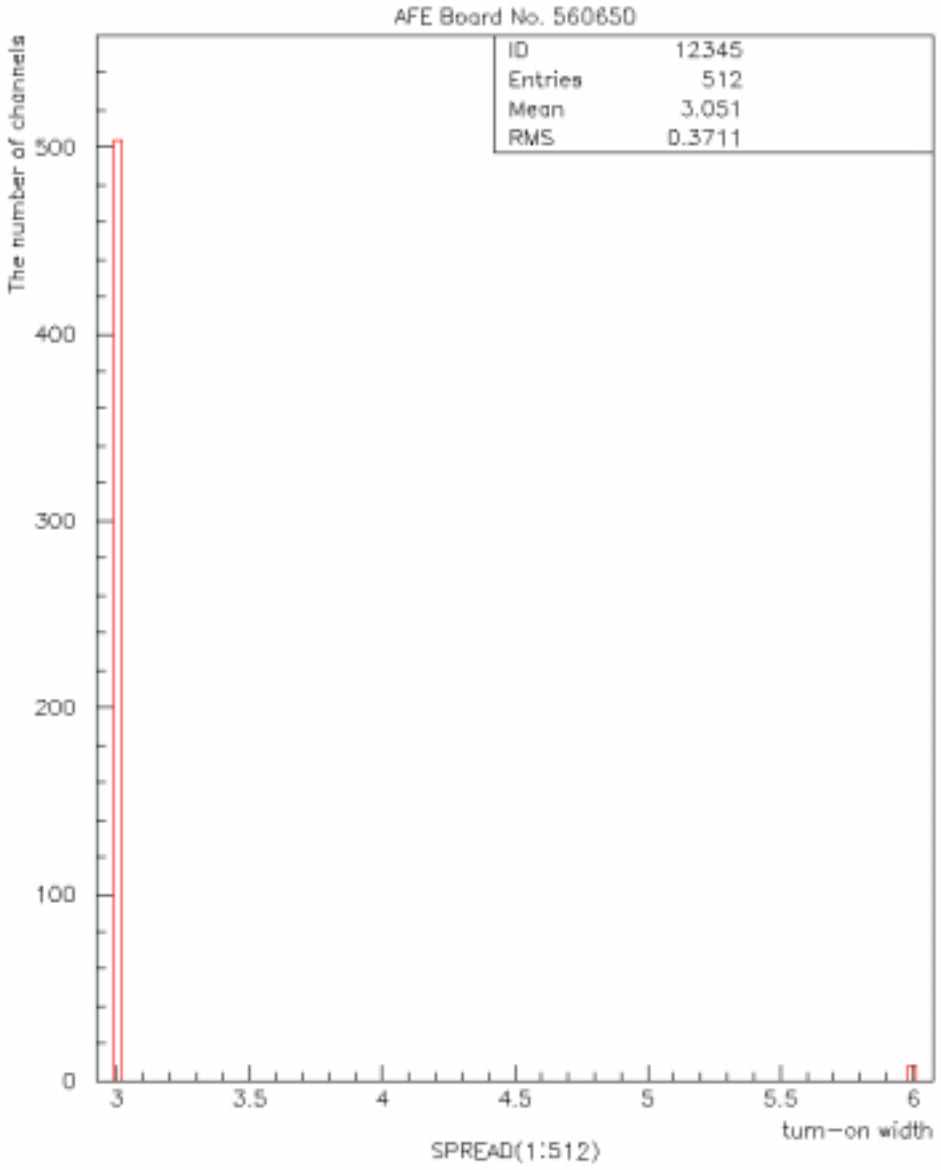


Fig. 34: Distributions of turn-on widths shown in Fig. 33.

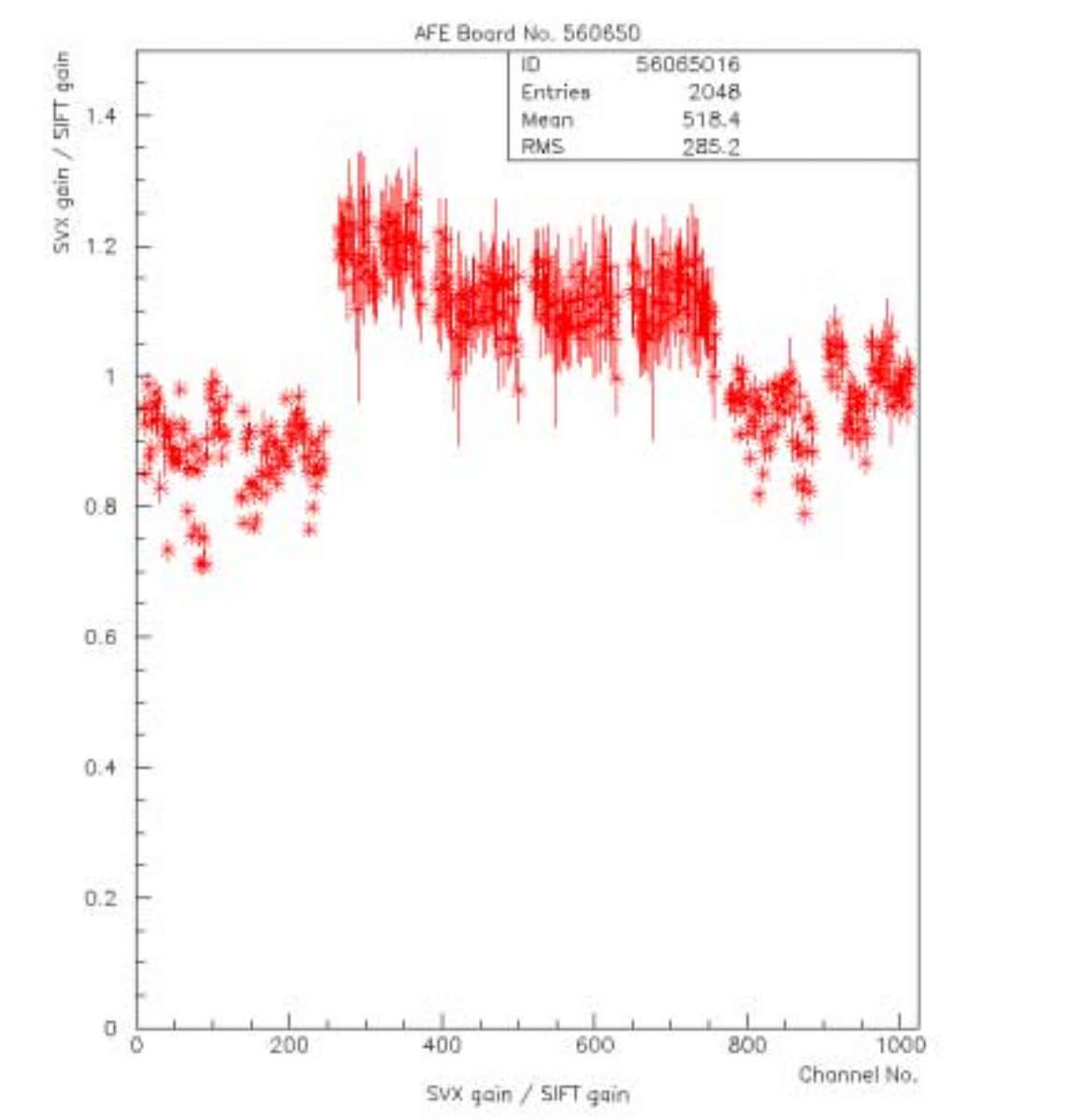


Fig. 35: Ratio of SVX gain to SIFT gain for all channels displayed as a function of channel number.

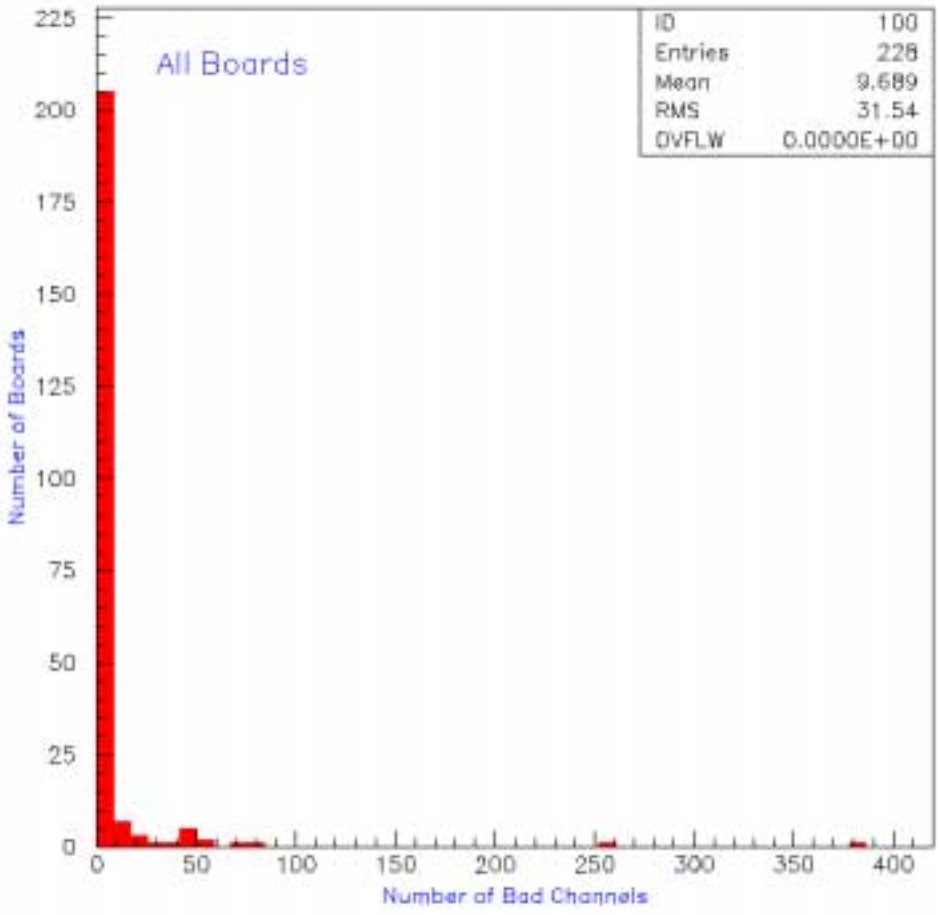


Fig. 36: Distribution of Number of bad channels for all AFE boards.

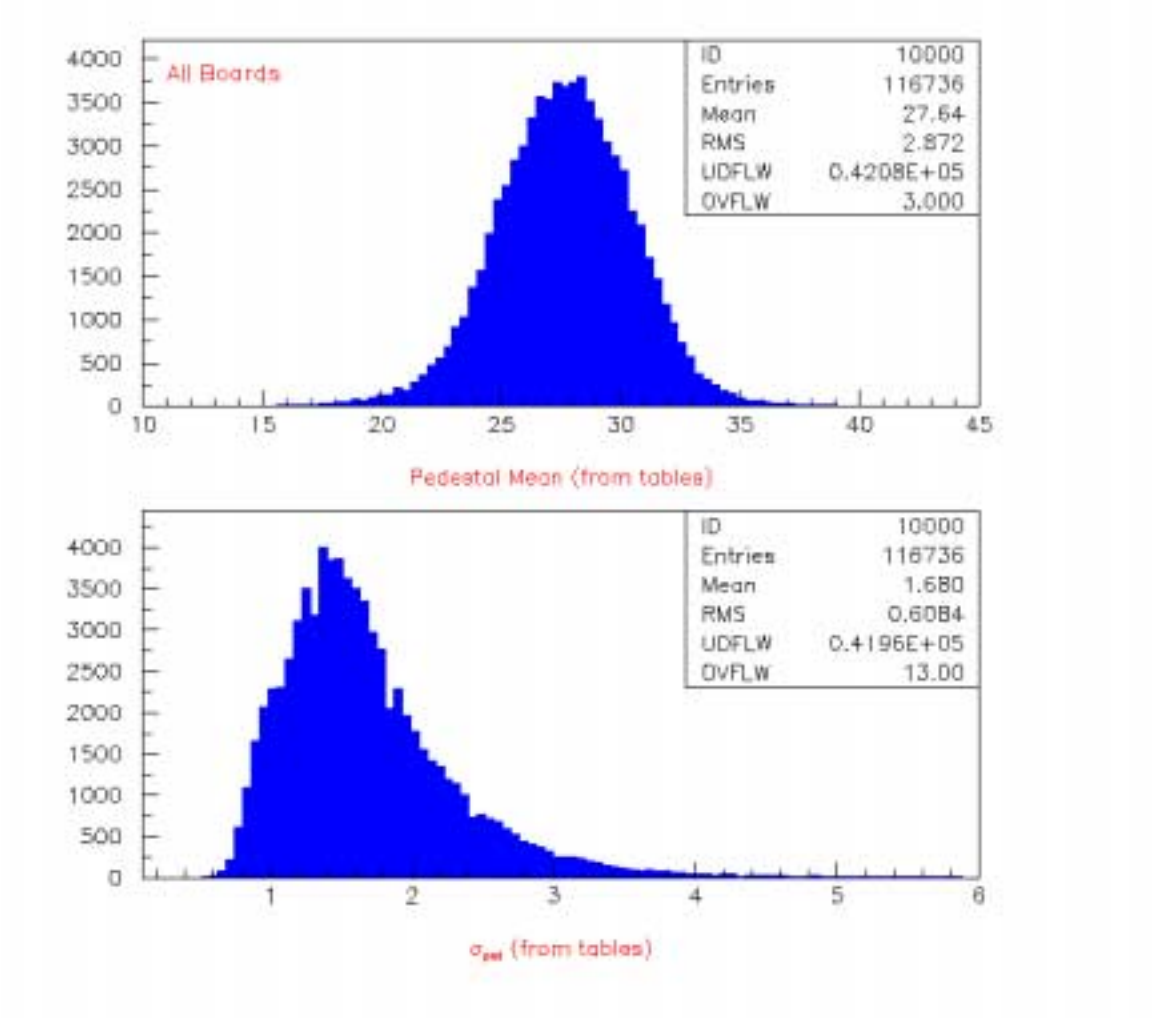


Fig. 37: Distribution of pedestals for all AFE boards.

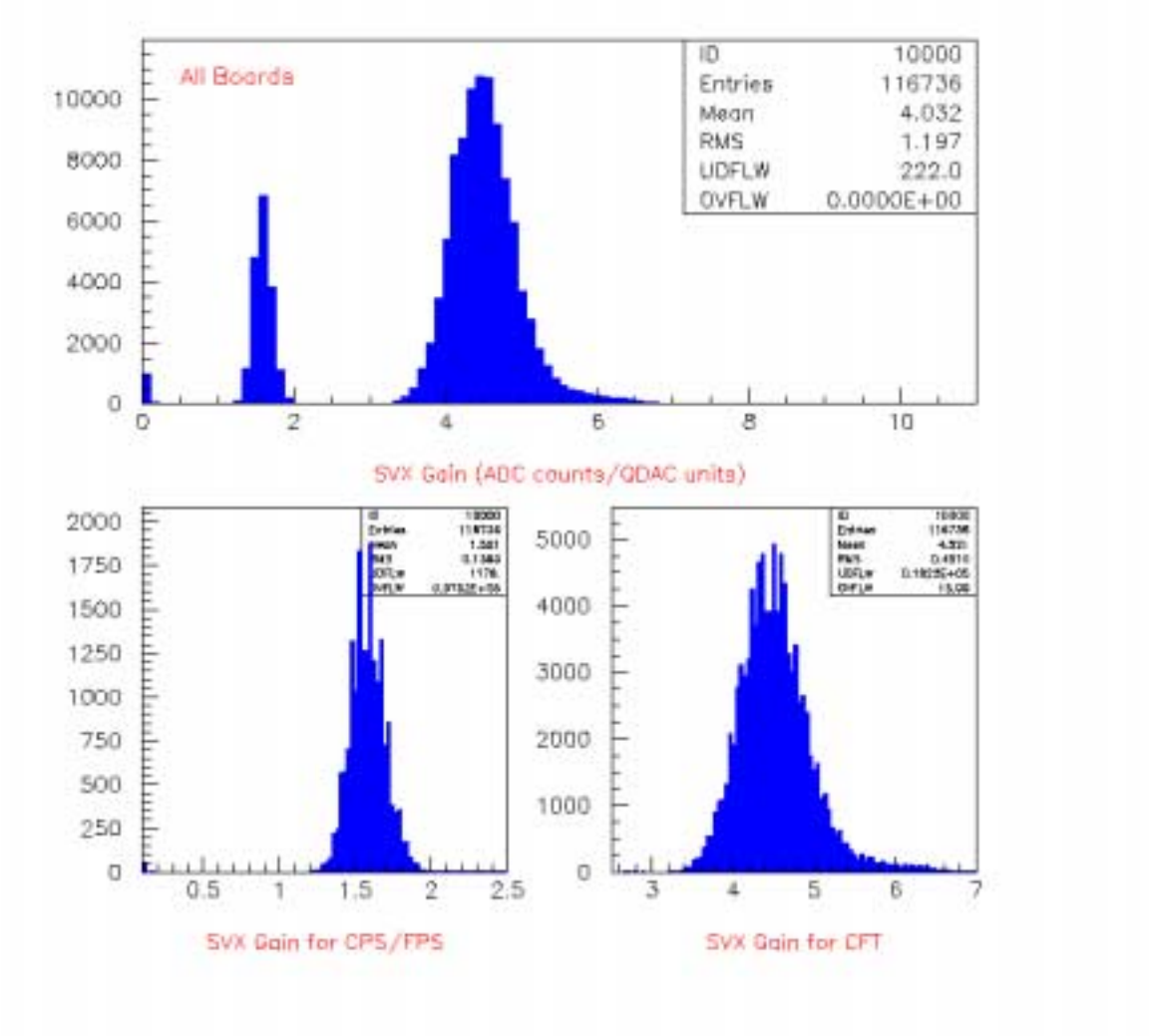


Fig. 38: (Top) Distribution of the SVX gain for all AFE boards. (Bottom) Plots show the SVX gain distributions for the CPS/FPS and the CFT boards.

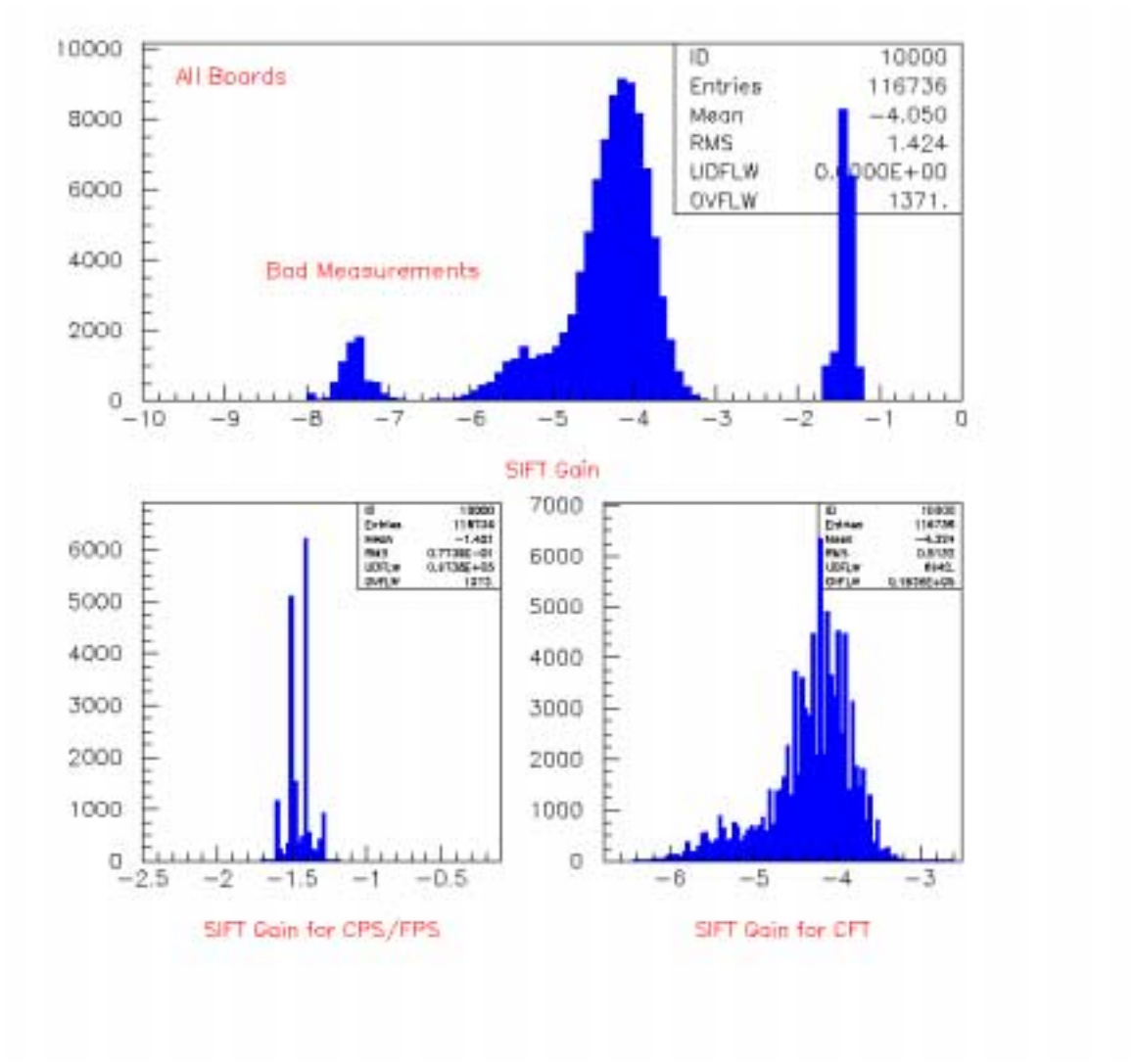


Fig. 39: (Top) Distribution of the SIFT gain for all AFE boards. (Bottom) Plots show the SIFT gain distributions for the CPS/FPS and the CFT boards.

References:

1. CFT Engineering Notes, John Anderson:
   http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/default.html
   In particular, see "D-Zero Central Fiber Tracker 8-MCM Analog Front End Board: Formal Design Specification"

2. AFE/DFE boards for Fiber Tracker, Jerry Blazey:
   http://d0server1.fnal.gov/users/blazey/afe/afe.html

3. AFE Board Phase-5 Testing, Pushpa Bhat:
   http://www-d0.fnal.gov/~pushpa/afe.htm

4. Index of /d0dist/dist/packages/afe_phase5
   http://www-d0.fnal.gov/d0dist/dist/packages/afe_phase5/